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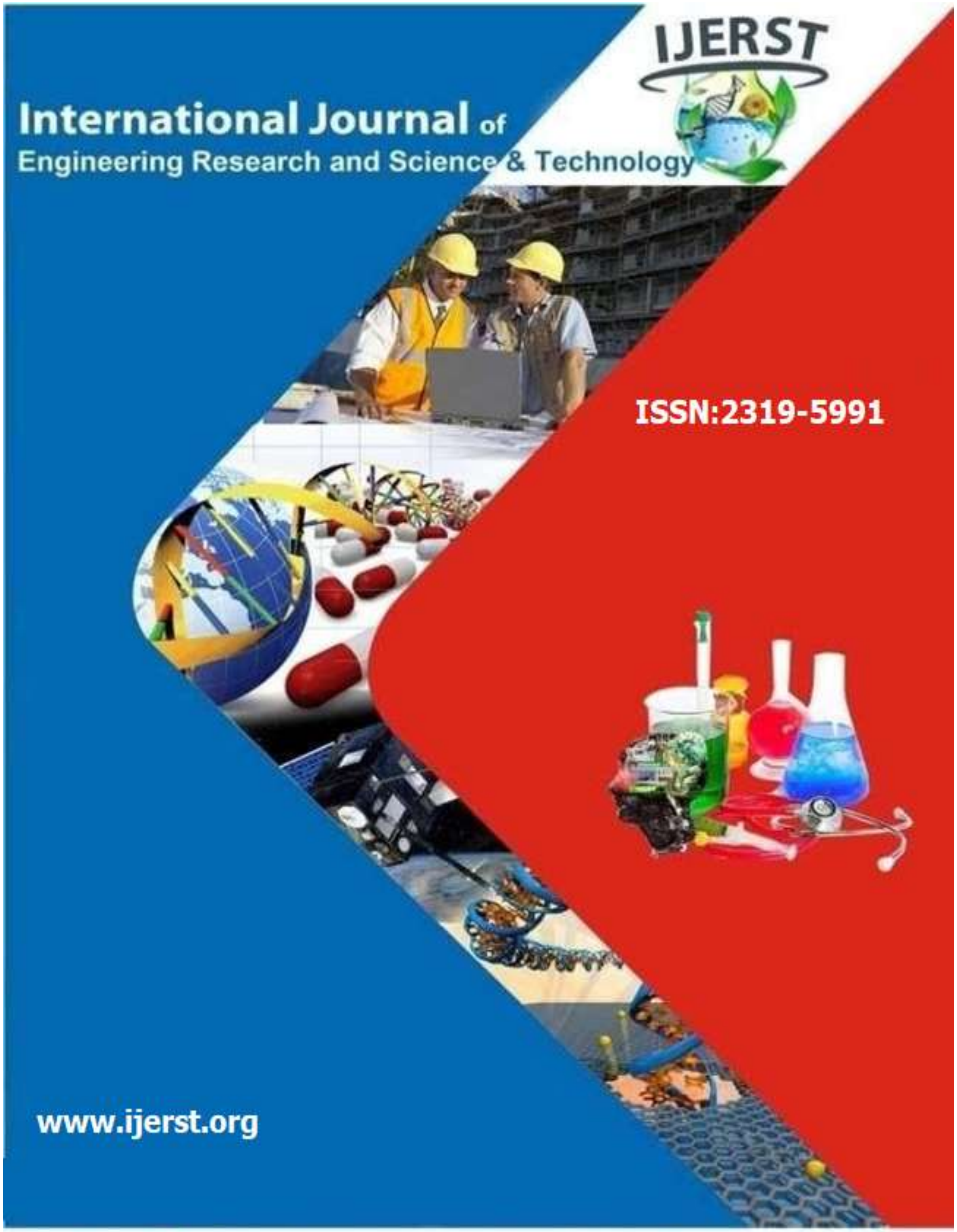

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DESIGN A COMPARATOR WITH LOW KICKBACK

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ABSTRACT

This brief presents a three-stage comparator and its modified version to enhance speed and Reduce kick back noise. Compared to conventional two-stage comparators, the proposed three-stage design introduces an additional amplification stage that increases voltage gain and significantly improves operational speed. While traditional two-stage comparators typically utilize pMOS input pairs in the regeneration stage, this three-stage design employs nMOS input pairs in both the amplification and regeneration stages, benefiting from higher carrier mobility to further enhance speed. In the modified version of the three-stage comparator,

A CMOS input pair is used in the amplification stage. This configuration effectively cancels out the kickback noise from the nMOS transistors through the opposing kickback of the pMOS devices. Additionally, the modified design incorporates an extra signal path in the regeneration stage, further boosting the comparator's speed. For accurate benchmarking, both the traditional two-stage and the proposed three-stage comparators were implemented using the same CMOS process. Measured results demonstrate that the modified comparator improves speed and reduces kickback noise by a factor of ten. Notably, these enhancements are achieved without increasing the input-referred offset or noise.

I. INTRODUCTION

1.1. Introduction

Comparators are fundamental components in a wide range of analog and mixed-signal systems, most notably in analog-to-digital converters (ADCs). Their performance directly influences the speed, resolution, and overall efficiency of ADC architectures, especially in high-speed, high-resolution successive approximation register (SAR) ADCs. In these applications, key performance metrics such as comparison speed, kickback noise, input-referred noise, and offset become critical factors. Among the commonly used comparator topologies, the Strong-ARM latch is well known for its advantages, such as zero static power consumption, rail-to-rail output, and rapid regeneration enabled by positive feedback.

However, Strong-ARM architecture also presents limitations. Its regeneration speed is restricted by a weak current source under the latch due to the V_{DD}/2 common-mode bias of the input pair. Additionally, multiple stacked transistors necessitate a higher supply voltage, posing challenges in low-voltage environments.

To overcome these issues, two-stage comparator designs have been explored. A notable example is Miyahara's comparator, which uses a separate preamplifier and regeneration latch to improve performance. This structure allows higher gate-source voltage across the latch input pair (V<sub>GS</ sub> ≈ V_{DD}), leading to faster regeneration and reduced supply voltage requirements due to fewer stacked transistors. Despite these improvements, the use of pMOS transistors in the latch stage of two-stage comparators still limits speed due to the lower hole mobility compared to electrons in nMOS transistors. This constraint motivates the

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need for an enhanced comparator structure that supports faster switching while minimizing kickback noise and maintaining low offset. In this context, the paper introduces a novel three-stage comparator architecture.

The proposed design incorporates an additional amplification stage between the preamplifier and latch, enabling the exclusive use of high-speed nMOS input pairs in both stages. This configuration boosts voltage gains and speeds up the regeneration process while also reducing the input referring to offset and noise.

1.2. Motivation

The motivation behind the research or design of "A Three-Stage Comparator and Its Modified Version with Fast Speed" generally stems from the ongoing need to improve performance, speed, and power efficiency in analogue and mixed-signal integrated circuits, especially Analog-to-Digital Converters (ADCs).

Here's a breakdown of the typical motivation behind such work:

1. Need for High-Speed Comparators

- Comparators are critical in high-speed ADCs (like flash ADCs).
- Traditional two-stage comparators (pre-amplifier + latch) may not meet speed requirements for gigahertz-range ADCs.
- A third stage can help amplify the signal faster and prepare for quicker decision-making in the latch.

2. Improved Gain and Bandwidth

- Adding an extra amplification stage allows:
  - o Higher overall gain before the regenerative latch.
  - o Better control over offset, noise, and common-mode rejection.
  - o Faster response to small input differences.

3. Trade-offs in Power and Area

- Designers seek ways to enhance speed without significantly increasing power consumption or area.
- A modified version of the three-stage comparator might address these trade-offs by optimizing biasing, transistor sizing, or using dynamic power-saving techniques.

4. Motivation behind Modified Version

- The modified comparator version could include:
  - o Dynamic latch enhancements for faster regeneration.
  - o Improved common-mode feedback control.
  - o Use of body biasing or digital calibration for offset trimming.

Summary of the Core Motivation:

To design a comparator with higher speed and better performance (gain, bandwidth, power efficiency), particularly suitable for high-speed ADCs, while addressing limitations of traditional two-stage comparators..

II. LITERATURE REVIEW

Low- Power High-Speed Comparator for Precise Applications

Khorami, A., & Sharif khani, M., 2018

This work presents a comparator architecture optimized for high-speed and low-power operations in precise analog circuits. The authors focused on minimizing propagation delay and offset voltage by introducing modifications to transistorizing, clock signal management, and current tail configurations. The comparator was implemented in CMOS 180-nm technology and demonstrated notable improvements in delay without a significant increase in power consumption.

However, the work primarily concentrates on general performance metrics and does not explore the issue of kickback noise, which is critical in high-speed ADCs. The proposed

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three-stage comparator in our work builds upon this foundation by not only targeting speed and power but also significantly reducing kickback noise using a CMOS input pair in the amplification stage

Analysis and Design of a Low-Voltage Low-Power Double-Tail Comparator Babayan-Mash hadi, S., & Lotfi, R.,2014

This paper introduces a double-tail comparator structure capable of operating at lower supply voltages while consuming minimal power. The architecture separates the pre amplification and regeneration functions using a two-branch structure, thus enabling independent optimization of speed and power. The design also addresses the metastability and offset concerns common in traditional latches.

Although the design offers good trade-offs between delay and power, it still faces limitations due to the use of pMOS transistors in the latch, which slows down regeneration because of lower hole mobility. In contrast, our proposed three-stage design leverages nMOS input pairs in both the preamplifier and latch stages to enhance speed. Additionally, the modified version reduces kickback noise, which the double-tail comparator does not explicitly address.

The Strong-ARM Latch [A Circuit for All Seasons] Razav I, B.,2015

The Strong-ARM latch is a well-known comparator to pology used extensively in ADCs due to its low power consumption and full-swing output. This paper reviews its working principle, which involves dynamic operation and regenerative feedback to quickly resolve input differentials. It is suitable for high- speed digital interfaces and ADCs.

Despite its efficiency, the StrongARM latch has limitations in regeneration speed because of its reliance on weak current sources and multiple stacked transistors. It also suffers from considerable kickback noise, which affects ADC accuracy. The three-stage comparator proposed in our work overcomes these drawbacks by incorporating extra gain stages and nMOS input pairs, and the modified version further introduces a CMOS structure to neutralize kickback, significantly improving upon the StrongARM architecture.

A1.2-V Dynamic Bias Latch-Type Comparator
in 65-nm CMOS With 0.4- mV Input Noise Bindra, H.S., Lokin, C.E., Schinkel, D., Annema, A.-J., & Nauta, B.,2018

This paper presents a latch-type comparator that achieves ultra-low input-referred noise (0.4 mV) by using a dynamic biasing technique. The dynamic biasing helps reduce power and offset low supply voltages. The design is implemented in 65-nm CMOS technology, making it suitable for modern ADCs where compact size and precision are important.

While the noise performance is impressive, the design still uses traditional regeneration structures that limit speed. Furthermore, kickback noise, which can corrupt sampled inputs in SAR ADCs, is not a key focus. In contrast, the modified three-stage comparator presented in our study directly addresses both noise and kickback by introducing signal path enhancements and complementary input devices.

A2.2/2.7fJ/ Conversion-Step10/12-bit40kS/s SARADC
With Data-Driven Noise Reduction Harpe, P., Cantatore, E., & van Roermund, A.,2013

This paper describes an ultra-low-energy SAR ADC with an innovative data-driven noise reduction method. Operating at 40 kS/s, the ADC achieves an energy efficiency of 2.2/2.7 fJ per conversion step. The role of the comparator is crucial in this design, as it directly impacts noise and conversion accuracy. However, the comparator used here is not optimized for high-

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speed operations or kickback noises up pression. In SAR ADCs, kickback noise from the comparator Cande grade resolution, particularly during the final bit decisions.

III. PROPOSED SYSTEM

The proposed system introduces a three-stage comparator, and a modified version designed to enhance speed, reduce kickback noise, and improve overall performance for high-speed, high-resolution analog-to- digital converters (ADCs). The system aims to address the key challenges in comparator design, including regeneration speed, noise, and offset, while maintaining low power consumption.

1.1. Three-Stage Comparator Architecture

The core innovation of the proposed system is the three-stage comparator. The design introduces an additional amplification stage between the preamplifier and the latch stage to enhance performance. The key features of this system are

- Three Stages of Operation: The system consists of three distinct stages, an initial preamplifier stage, a secondary amplification stage, and a final regeneration (latch) stage. Each stage plays acrolein boosting performance while maintaining high fidelity.
- **nMOS Input Pairs:**

Unlike conventional two-stage comparators, which often rely on pMOS transistors in the regeneration stage, the three-stage comparator employs nMOS input pairs in both the regeneration and amplification stages. This configuration leads to higher regeneration speeds and better performance due to the superior electron mobility of nMOS transistors.

- **Voltage Gain:**

The extra amplification stage provides a significant voltage gain, which helps enhance the speed and accuracy of the comparator. This amplification also aids in reducing input-referred noise and offset, improving overall comparator reliability.

- **Improved Signal Settling:**

With the addition of the extra preamplifier stage, the comparator achieves faster signal settling at the output nodes, resulting in quicker response times. This is particularly beneficial for high-speed ADC applications where time resolution is crucial.

1.2. Modified Three-Stage Comparator

In addition to the standard three-stage comparator, a modified version is proposed to address kickback noise, which is often a significant problem in high-speed comparator designs. The main differences and improvements in the modified version are:

CMOS Input Pair in the Amplification Stage: The amplification stage in the modified version uses a CMOS input pair, combining pMOS and nMOS devices. This helps cancel the kickback noise generated by the nMOS devices, significantly reducing the total kickback noise produced during operation.

Extra Signal Path in the Latch Stage: To further improve speed and reduce noise, an extra signal path is introduced in there generation(latch) stage . This path provides additional signals that speed up the regeneration process, enhancing the overall speed of the comparator while maintaining low input-referred offset and noise.

Kickback Noise Reduction: The combination of the CMOS input pair and the extra signal path leads to a tenfold reduction in kickback noise. This is particularly beneficial for applications that require high resolution and precision, such as SAR ADCs.

1.3. Circuit Design and Implementation

The three-stage and modified comparators are implemented using a 130-nm CMOS process, ensuring compatibility with modern ADC designs. The system is designed to operate efficiently while maintaining high speed and low

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power consumption. The key design considerations include:

- **Transistor Sizing:**

To achieve the desired performance, the input pair transistors for each stage are sized appropriately. The transistor width/length ratios (W/L) are optimized to ensure that the input referred noise is minimized, and the regeneration speed is maximized.

- **Clocking and Reset Mechanism:**

The comparator features an optimized clocking scheme that ensures proper synchronization between stages. The reset mechanism ensures that the system operates without static current during idle periods, contributing to power efficiency.

- **Power Consumption and Speed Trade-offs:**

While the three-stage comparator requires more power than a two-stage comparator due to its added complexity, the system's speed and noise performance justify this trade-off. In comparison, the two- stage comparators cannot achieve the same speed even with higher power consumption, due to their inherent limitations in signal regeneration speed and noise control.

IV. ADVANTAGES

A three-stage comparator is an advanced type of comparator circuit used primarily in analog and mixed- signal systems (like ADCs – Analog to Digital Converters). It typically includes three stages: a preamplifier, a decision-making stage (positive feedback or latch), and an output buffer. Here are the key advantages of a three-stage comparator:

4.1. Advantages of three-stage comparator

➢ **High Accuracy**

Preamplifier stage reduces offset and noise from the input signal before it is fed to the latch, improving overall precision.

➢ **Fast Switching Speed**

The latch or regenerative stage rapidly amplifies small differences to a full logic level, allowing for quick decision-making even with small voltage differences.

➢ **Low Input Offset**

The multi-stage design, especially with a preamp, minimizes input offset voltage which is critical for high-resolution applications.

➢ **Improved Noise Performance**

The preamplifier helps filter out high-frequency noise, enhancing the comparator’s robustness in noisy environments.

➢ **Isolation Between Stages**

Each stage is optimized for a specific task (sensitivity, speed, or drive strength), reducing loading effects and allowing better performance tuning.

➢ **High Gain**

The cumulative gain across stages helps detect very small input differences and produce reliable digital outputs.

➢ **Scalability**

This structure is commonly used in high-speed ADCs (e.g., flash ADCs), making it ideal for applications requiring scalability and modularity.

4.2. Disadvantages

➢ **Increased Power Consumption**

Having multiple stages (preamplifier, latch, and output buffer) leads to higher power usage compared to simpler, single-stage comparators.

➢ **Larger Chip Area**

The three-stage structure requires more transistors and routing, increasing the silicon area, which can be a drawback in compact or low-cost designs.

➢ **Higher Design Complexity**

The need to optimize and match each stage (especially for gain, timing, and offset) makes the design more complicated and time-consuming.

➢ **Longer Propagation Delay**

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While the latch itself is fast, the overall signal must pass through three stages, which can increase the total delay compared to simpler comparators.

- **Potential Stability Issues**

Multiple stages, especially with high gain and feedback, can introduce stability or oscillation problems if not carefully designed.

- **Sensitivity to Mismatch**

Any device mismatches in the preamp or latch can significantly affect offset voltage and accuracy, especially in high-resolution applications.

- **Calibration Needs**

Due to increased offset and mismatch possibilities, some designs require offset correction or calibration circuitry, further complicating the system.

4.3. Applications

- **Analog-to-Digital Converters (ADCs)**

Flash ADCs and pipelined ADCs use arrays of high-speed three-stage comparators to quickly convert analog signals into digital form with high resolution.

- **High-Speed Data Acquisition Systems**

Used in systems that require fast and accurate signal sampling, such as oscilloscopes, radar systems, and digital communication receivers.

- **Wireless Communication Devices**

Helps in signal detection and comparison in RF front ends and demodulators, where low latency and high accuracy are essential.

- **Image and Video Processing Systems**

Employed in sensors and processors for pixel-level comparisons, particularly in CMOS image sensors and high-frame-rate cameras.

- **Precision Measurement Instruments**

Utilized in digital voltmeters, signal analyzers, and test equipment for fine voltage comparison tasks.

- **Industrial Control Systems**

Used in control and automation circuits where high-speed threshold detection and decision-making are critical.

- **Medical Electronics**

Applied in devices like EEG, ECG, and imaging systems, where reliable and fast analog signal processing is needed.

- **High-Speed Memory Circuits**

Acts as a sense amplifier or comparator in read/write operations for SRAM or flash memory arrays

V. CONCLUSION AND FUTURE SCOPE

CONCLUSION

In this work, we proposed a novel three-stage comparator and its modified version to address key challenges in high-speed, high-resolution analog-to- digital converters (ADCs). The introduction of an additional amplification stage between the preamplifier and regeneration latch significantly improves the speed and performance of the comparator.

By utilizing nMOS input pairs in both the amplification and regeneration stages, we achieve faster signal settling and reduced input-referred noise, thereby enhancing overall comparator efficiency.The modified version further improves performance by incorporating a CMOS input pair in the amplification stage to cancel kickback noise.

The addition of extra regeneration paths in the latch stage accelerates the decision- making process, reducing regeneration time and increasing the comparator’s speed by 32%. Moreover, the modified design results in a tenfold reduction in kickback noise compared to traditional two-stage comparators.

Post-layout simulations and experimental results show that the proposed three- stage comparator outperforms conventional two-stage designs in terms of speed, noise suppression, and off set reduction, making it highly suitable for high-

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speed, high-resolution ADC applications. These improvements demonstrate that the proposed system is an effective solution for next-generation ADC designs, providing enhanced performance without compromising on power consumption or accuracy. Overall, the three-stage comparator and its modified version offer a compelling design choice for high-speed, high-precision applications in digital signal processing and communication systems, paving the way for more efficient and accurate ADCs in modern electronic systems.

FUTURE SCOPE

As technology advances and demands faster, more precise, and energy-efficient systems grow, three-stage comparators—especially modified high-speed versions—are expected to play a critical role in the following areas:

a. **Next-Generation ADCs**
   - Trend: Increasing bit resolution and sampling rates (e.g., >1 GS/s).
   - Scope: Modified comparators with faster regeneration and lower offset will be vital in high-speed flash, pipelined, and time-interleaved ADCs used in 5G/6G, high-resolution imaging, and scientific instrument

b. **5G/6G & IoT Communication Systems**
   - Trend: Demand for low-latency and high-accuracy RF signal processing.
   - Scope: Comparators with enhanced latch speed and reduced decision time will
   - support high-throughput RF receivers, demodulators, and analog front ends in future wireless infrastructure.

c. **AI and Edge Computing Hardware**
   - Trend: AI chips require fast and low-power analog interfaces for sensory data.
   - Scope: Modified three-stage comparators with low power and high speed are ideal for edge inference processors, neuromorphic systems, and mixed-signal AI accelerators.

d. **Biomedical Devices**
   - Trend: Real-time monitoring and wearable diagnostics.
   - Scope: Future comparators must be ultra-low power and accurate, making enhanced three-stage
   - Designs suitable for ECG, EEG, and implantable sensors.

e. **Low-Power, High-Speed Design in Sub-10nm Technologies**
   - Trend: Shrinking process nodes (e.g., 7nm, 5nm, 3nm).
   - Scope: Modified comparators must address process variations, leakage, and noise challenges, possibly using dynamic, digital-assisted, or calibration-enhanced architectures.

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