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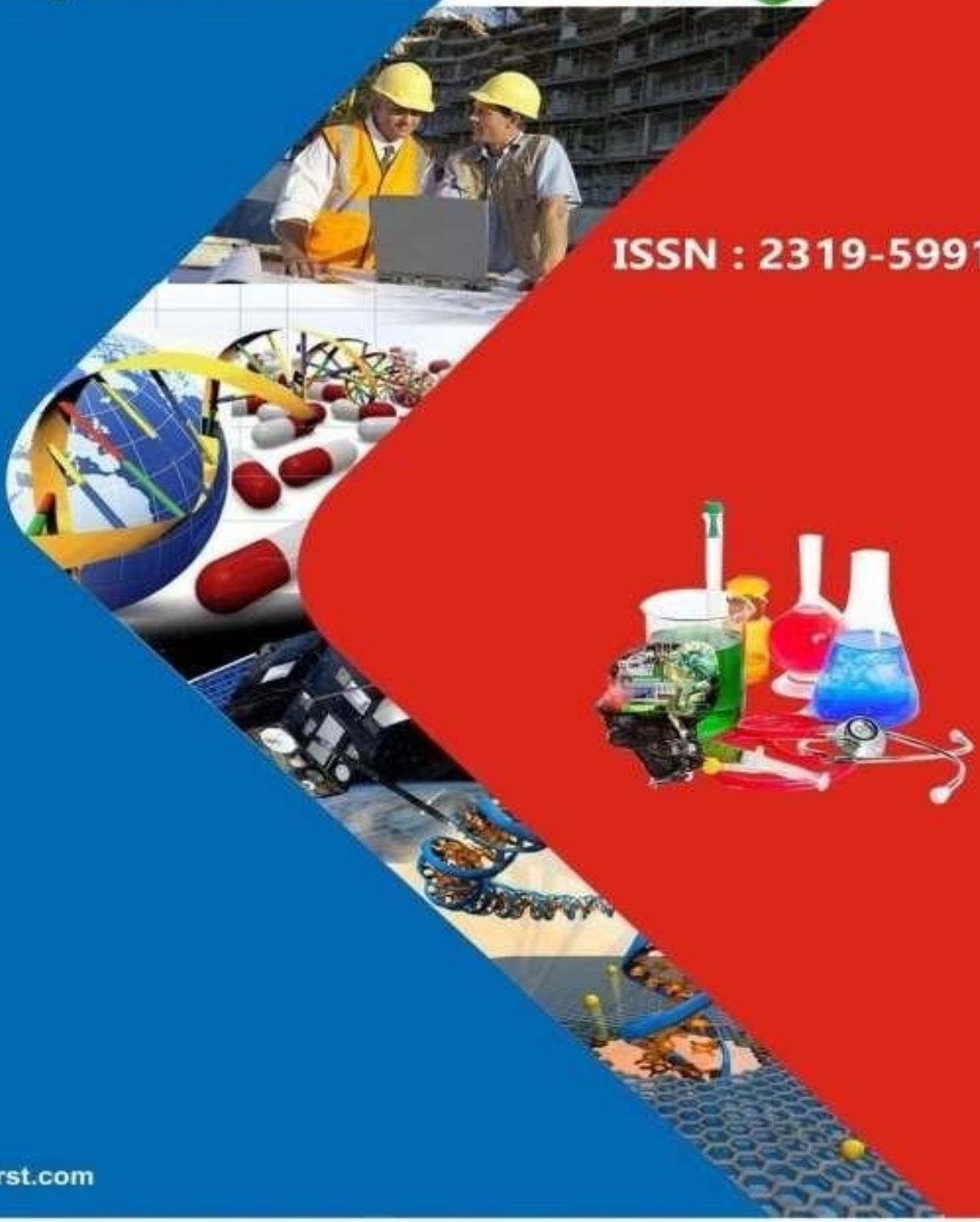

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Design and Implementation of Systolic Multiplier Using Hybrid Multiplexer Dependent Adder

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Abstract:
The implementation of a systolic multiplier using a hybrid multiplexer-dependent adder offers significant improvements in computational speed and efficiency, particularly in VLSI front-end design. According to recent studies, the global digital signal processing(DSP)marketisexpectedto reach$25.37billionby2026, growing at a compound annual growth rate (CAGR) of 9.4%. Multipliers are fundamental components in DSP systems, and efficient multiplier designs are critical for enhancing performance, especially in real-time applications. However, traditional multiplier designs, like Baurn and Wallace multipliers, suffer from high power consumption, increased latency, and complex architectures that make them unsuitable for modern VLSI applications. In this work, we propose a novel systolic multiplier that leverages a multiplexer-dependent adder composed of a 2-to-1 multiplexer and a full adder. This design is further enhanced by integrating a systolic array architecture and a Razor Flipflop for error detection and correction. The use of a multiplexer-dependent adder reduces the overall complexity of the multiplier, while the systolic array ensures high-speed parallel processing. The Razor Flipflop provides error tolerance, enabling the system to maintain performance undervariable operating conditions. This novel combination significantly improvesspeed,reducespowerconsumption,andenhancesreliability in VLSI implementations.

Keywords: Systolic Multiplier, Hybrid Multiplexer, VLSI- Very large scale Integration, Digital Signal Processing, BaurnMultiplier, Wallace Multiplier, Razor Flipflop, Reliability.

1. INTRODUCTION

In the ever-evolving landscape of VLSI design, the pursuit of innovative architectures for efficient multiplication has become increasingly pivotal. Systolic multipliers, characterized by their parallel computing capabilities, offer a promising avenue to meet the escalating demands for high-throughput arithmetic operations. This paper introduces a novel approach to systolic multiplier design, incorporating a hybrid multiplexer-dependent adder. The motivation behind this hybridization lies in addressing the challenges posed by traditional multiplication methods, aiming to strike adelicate balance between computational speed, area utilization, and power efficiency.

Conventional multiplier architectures grapple with the challenge of reconciling the need for faster computation with the constraints imposed by limited silicon real estate and power budgets. Systolic arrays, which enable parallelism in data processing, present an opportunity to transcend these limitations. The motivation for this research stems from a desire to optimize systolic multipliers.

This innovative design not only capitalizes on the inherentadvantages of parallelism in systolic arrays but also seeks to streamline the critical path through the integration of a flexible and efficient adder structure. This study is guided by two primary objectives. First, to devise a systolic multiplier that effectively exploits the parallel processing paradigm to achieve rapid multiplication. Second, to seamlessly integrate a hybrid multiplexer-dependentadderintothesystolicarray,therebyoptimizingthecritical path andminimizingoverall latency.Thehybridadder, enrichedwith multiplexer-based components, introduces a versatile and efficient mechanism for addition within the systolic multiplier. By pursuing these objectives, this research aspires to contribute significantly totheongoingadvancementsinVLSIdesign,pushingtheboundariesof computational efficiency in digital signal processing and other relevant applications.

Theresearchobjectivesforimplementingasystolicmultiplierusinga hybrid multiplexer-dependent adder in VLSI involve optimizing computational efficiency, minimizing area utilization, and reducing power consumption. The study aims to enhance the flexibility and versatilityofthehybridadderwithintheparallelprocessingparadigm of systolic arrays.Additionally, it explores the algorithmic suitability of the hybrid approach, assessing its fault tolerance and reliability. Comparative performance analysis against existing multipliers with different adder architectures is conducted, along with a focus on scalability, integration, and the exploration of design trade-offs for achieving an optimal balance between area, power, and speed inVLSI designs.

2. LITERATURESURVEY

Sadhineni, Harika, S. Josaph,et.al [1] proposed this paper, we designed the CMOS based multiplier using LFSR for high-speed operation. Basically, the memory cells, multidimensional memory circuits and memory frameworks were referenced with various sub-chips. The main intent behind using an Linear Feedback ShiftRegister (LFSR) Controller was to provided full speed operations.The proposed architecture planned full-speed activity of some non-straight calculations that were winded up increasingly more significant in present day memory testing, conclusion. The combinational logic and scan logic provides a solution to the system in a specified manner. Compared to existed design, the proposed system gives effective results.

Srinivas, Chundi Sai, M. S. Manohar,et.al [2] discussedmain objective of this research article was to designed high efficient accurate DL-PO logic multiplier for low power applications. primarily, the execution of DL-PO Multiplier was based on VLSI chips, which were used as critical element. In the multiplier, product information was utilised to create the propagator and generatorsignals in the same way. While designing the dual partial productunit, optimized multiplier were used most widely. The DL-PO logic Multiplier uses adequate hardware implemented. The DL-PO logic depended on Multiple selection logic module (MSLM). Hence compared to state-of-the-art system, the DL-PO logic Multiplier systems gives effective results in terms of speed, area and delay.

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Kim, Sunwoong, Cameron J. Norris,et.al [3] discussed IEEE 754 standard for floating-point (FP) arithmetic was widely used for real numbers. Recently, a variant called posit was proposed to improvethe precision around 1 and −1 . Since FPmultiplication requires high computational complexity, various algorithmic approaches and hardware accelerator solutions were explored. Here, this article proposes a novel area-efficient logarithmic multiplier architecture for different real number formats, which also provides a significant and useful accuracy/latency tradeoff at runtime. To reduce the logic area in field-programmable gate arrays (FPGAs), this article offers two innovations: applying logarithm to only a single operand and mitigating the accuracy drop caused by this modification with advanced error converging and operand selection schemes. Our multiplier design for single-precision FP (SPFP) numbers uses 58% fewer hardware resources than the iterative Mitchell's multiplier (IMM) design of Babić et al. extended for SPFP numbers. The error falls within 0.5% when the number of iterations reaches 5. In JPEG, our SPFP multiplier with four iterations produces nearly identical image quality results to the conventional exact multiplier.We further show how to merge two SPFP multipliers for double-precision FP (DPFP) multiplication. This DPFP multiplier design reduced the hardware resources of the IMM design extended for DPFP numbers by 60%. Finally, we demonstrate how our SPFP multiplier designwas slightly modified for 32-bit posit multiplication. It achieves a significantly higher accuracy by increasing the number of iterations compared to state-of-the-art approximate posit multiplier designs.

Minaeifar, Atefeh, Ebrahim Abiri,et.al [4] observed multipliers were most frequently employed components in a system, responsible for performing computations, while significantly contributing to power consumption. In that article, a new architecture was presented by removing the least significant bits to implement three multipliers (Mul-1, Mul-2, and Mul-3) with the aim of reducing complexity and power consumption. Mul-1 demonstrated the highest accuracy along withlowenergyconsumptioncomparedtopreviousworks,achieving a favorable trade-off between accuracy and energy consumption.All proposed designs and existing multipliers were simulated and compared in 7 nm FinFET technology using the Hspice tool. Additionally, the accuracy and quality of the proposed approximate multiplierswereevaluatedusingMATLAB.Theresultsindicatedthat Mul-1 and Mul-3 were highly efficient in image processing applications. According to the findings, Mul-1 surpassed its counterpart by 10%, 50%, and 50% in terms of PDP, NMED, and MRED, respectively. Furthermore, Mul-3 exhibited satisfactory MSSIM in DSP applications, outperforming its counterpart by 23% and 16% in PDP and MRED. Meanwhile, Mul-2 improved PDP by nearly 53% compared to Mul-1 and had the lowest power consumption.

Hui, Yajuan, Qingzhen Li, LeiminWang,et.al [5] proposed In- memory computing represents an efficient paradigm for high- performance computing using crossbar arrays of emergingnonvolatile devices. While various techniques have been emerged to implement Boolean logic in memory, the latency of arithmetic circuits, particularly multipliers, significantly increases with bit- width. In this work, we introduce an in-memory Wallace tree multiplier based on majority gates within voltage-gated spin-orbit torque (SOT) magnetoresistive random access memory (MRAM) crossbar arrays.By utilizing a resistance sum, the majority gate is implementedduringREADoperationsinvoltage-gatedSOT-MRAM crossbar arrays, resulting in reduced read currents and improved energy efficiency. We employ a series of READ and WRITE operations to perform multiplier calculations, leveraged the fast READ and WRITE speeds of voltage-gated SOT-MRAM devices. Furthermore, the use of five-input majority gates simplifies multiplication by employed uniform logic gates and reducing logic depth, thereby lowering the operation's complexity and the total number of occupied cells. Our experimental results demonstrate that the proposed in-memory Wallace tree multipliers consume threetimesless energy for in-memory operations thanpreviously reported4×4multipliers.Moreover,theproposedmethodreducesthedelay overhead fromO (n2) to O (log2n), where n represents thenumber of bi.

Parmar,Rushik,KhushilYadav,GauraangiAnand,et.al[6]introduced myocardial infarction (MI) was a cardiac abnormality in which the coronaryarterygetsblocked,causingmillionsoffatalitieseveryyear. MI has a very high mortality and disability rate; therefore, with the detection of MI, it was also imperative to determine the location ofthe blockage to provide on–time treatment to avoid any fatality. In this paper, for the first time, a VLSI architecture was proposed that can determine the location of the infarction in real-time. Theproposed architecture classifies the electrocardiogram (ECG) into twelve classes and achieves an average accuracy, sensitivity, and specificity of 99.90%, 99.49%, and 99.94%, respectively. Its area utilization is 1.69 mm2 at SCL 180 nm Bulk CMOS technologynode, and the power consumption was 268.9 μW at 250 KHz. Thelow area and power requirements and real-time classification capability make the classifier suitable for wearable devices.

Beura, Srikant Kumar, SudeshnaManjari Mahanta, et.al [7]proposed inexact computing, was a modern approach for the development of low power and high-performance digital circuits, which involves approximation stages to get the utmost accurate result and are very much applicable in some error-tolerant applications like image processing. Such applicationswere limited to human eyesight ability, which given us the freedom to make the approximate output. In this manuscript, two inexact partial product generators, viz.Namely IPPG1, IPPG2 were proposed for the design of radix-4 based 8 × 8 Booth multipliers IRBM1.1, IRBM1.2, respectively. Moreover, an inexact 4:2 compressorwas also proposed to add such partial product bits generated by IPPG1 and IPPG2, and they were nomenclate as IRBM2.1 and IRBM 2.2, respectively. IPPG1 and IPPG2 were designed by introducing errors in the Karnaugh's map to reduce the circuit complexity and errors, respectively. Similarly, errors were introduced in the truth table of the exact 4:2 compressor to design a low power, high speed inexact 4:2 compressor. Error metrics estimation of such proposed inexact Booth multipliers and the state- of-the-art designs are performed using MATLAB and circuit performance parameters like area, computational delay and power dissipation are extracted using gpdk45 nm technology. While comparing, IRBM1.2 offers minimum error metrics than all other reported design so far. Moreover, in the circuit level prospect, IRBM1.1 consumes minimum power and IRBM2.2 is the fastest among its reported counter-parts. IRBM2.2 offers minimum power- delay-area (PDA) product over all of its reported counter-parts. For thevalidationoftheproposeddesigns,animagemultiplication,edge- detection using Sobel operator, and convolutional neural network- based application was incorporated and quality assessmentparameters are measured using MATLAB.

Vakili, Bahareh, Omid Akbari,et.al [8] introduced Approximate computing was one of the promising techniques in error-resilient applications to overcome high-density integration challenges, suchas energy consumption and performance. Multipliers constitute a significant portion of computer arithmetic units, leading to considerable energy and time consumption. In this paper, low-power and compact approximate compressors were proposed for composing approximate Dadda multiplier structures, including compressors,half adders, and full adders, which utilize three-phase partial product compression: truncated, approximation, and exact columns. In approximate columns,approximate compressors were considered, derived from the truth table of the exact 4:2 compressor and simplified K-map entries based on the probability of each combination of inputs. An error-correcting module (ECM) was designed to distinguish specific cases and reduce the error metrics.All circuits were simulated using we conducted image multiplication and implemented a simple multi-layer perceptron (MLP) neural network using the modified National Institute of Standards and Technology (MNIST) dataset in MATLAB with 0.998 mean structural similarity index metric (MSSIM), 51 dB peak-signal noise ratio (PSNR), and 95% classification accuracy.

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3. PROPOSEDMETHODOLOGY

In the realm of VLSIdesign, the development of efficient and high-performance multipliers is a critical aspect, particularly inapplications such as digital signal processing, graphics processing, andvariouscomputationaltasks.Oneinnovativeapproachtoenhance the efficiency of multipliers is the utilization of systolic architectures coupled with hybrid multiplexer-dependent adders. This integration aims to optimize both speed and area utilization, addressing the ever- increasing demand for faster and more power-efficient circuits.

Systolic architectures, inspired by the human cardiovascular system, are designed to achieveparallelism and pipelining in data processing. They are characterized by a regular grid of processing elements that collaboratively compute and propagate results through a structured flow of data. When combined with hybrid multiplexer-dependent adders, which intelligently select and combine different addition techniques based on the operands, these systolic multipliers can deliver superior performance in terms of speed and area efficiency.

The hybrid multiplexer-dependent adder introduces flexibility in selecting the most suitable adder architecture for a specific set of operands. This adaptability enables the systolic multiplier to dynamically adjust its operation based on the characteristics of the input data, minimizing the overall delay and power consumption.

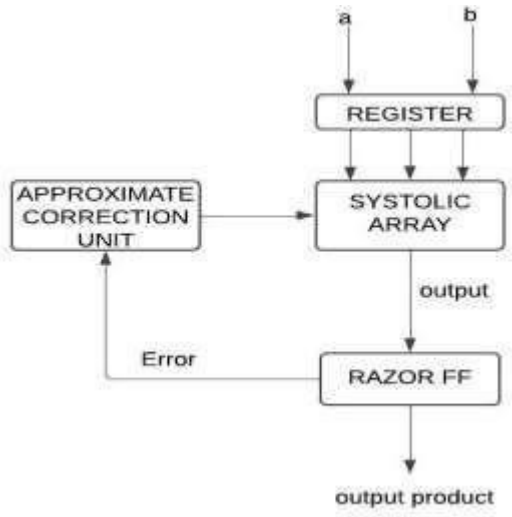

Figure1:ProposedSystolicMultiplier.

Thedetailed systolicmultiplier isgivenas follows

Processing Elements (PEs): PEsarethefundamental computing units within the systolic array. Each PE performs basic arithmetic operations, typically involving multiplication and addition. PEs are arranged in a regular grid or array configuration.

Registers: Registers are used for storing intermediate results and operands. Each PE has its local registers, providing a temporary storage space for data during the computation process. Registers enable the pipelined flow of data through the systolic array.

Systolic Array Operation: The systolic array is initialized with input operands. Data flows through the array in a coordinated, systolic manner. Each PE performs a specific computation on the data it receives and passes the result to its neighbouring PEs. This pipelined and parallel approach allows for efficient multiplication.

Razor Flip-Flops: Razor flip-flops are a type of flip-flop circuit designed to operate at lower supply voltages, enhancing energy efficiency.Inasystolicmultiplier,razorflip-flopsbeemployedas storage elements within each PE. These flip-flops contribute to the overall energy-efficient design of the systolic multiplier.

ApproximateCorrectionError:Approximatecorrectionerrorrefersto the potential inaccuracies introduced during the approximate computation in systolic multipliers. As systolic multipliers use approximations to reduce power consumption or improve speed, errorsoccur in the computed results.Techniques for correcting these errors involve employing error detection and correction mechanisms. Approximate correction error mitigation strategiesinclude error- tolerant algorithms, redundancy, or feedback loops to refine the results.

A systolic multiplier is a specialized hardware component used for rapid multiplication of largenumbers, commonly employed in digital signal processing applications. It operates within a systolic array architecture, where data flows through a grid of interconnected processing elements. Each element conducts partial multiplicationand addition operations, with results cascading to adjacent elements, facilitating parallel computation. This arrangement enables efficient handling of repetitive multiplication tasks such as matrix multiplication and digital filtering. Systolic multipliers offer notable advantages in terms of speed and efficiency compared toconventional methods, making them valuable for various computational tasks. They are often implemented in dedicated integrated circuits like ASICs or FPGAs to achieve optimized performance across different computing applications.

Applications:

Theapplicationsofproposed systemaregiven asfollows

- DigitalSignalProcessing(DSP)
- WirelessCommunicationSystems
- Cryptographic Systems
- ScientificComputing
- ArtificialIntelligenceandMachine Learning
- EmbeddedSystems
- DigitalImageandVideoProcessing
- BiomedicalSignalProcessing: **Advantages:**

Theadvantagesofproposedsystemaregiven as follows

- Enhanced Computational Speed: The hybrid multiplexer-dependent adder, integrated into the systolic multiplier, can contribute to accelerated multiplication operations. This resultsinincreased computationalspeed,making itsuitable for applications where rapid arithmetic processing iscrucial.
- Optimized Critical Path and Reduced Latency: By leveraging the flexibility of the hybrid adder, the critical path in the systolic multiplier was optimized, leading to reduced latency in multiplication operations. This improvement in timing characteristics enhances overall system performance.
- BalancedTrade-offs BetweenArea, Delay, andPower:The hybrid approach aims to strike a balance between the complexitiesassociatedwithtraditionaladderarchitectures, offering a potential reduction in area utilization while maintaining or improving powerefficiency.This balance is crucial for meeting the stringent requirements of modernVLSI designs.
- Versatility in Handling Multiple Operations: The hybrid multiplexer-dependent adder can provide versatility in handling various computational scenarios, contributing to the efficient execution of multiple operations within the systolic multiplier. This adaptability is advantageous for applications requiring diverse arithmetic computations.

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- Increased Parallelism in Systolic Arrays: Systolic multipliers inherently rely on parallel processing. The hybrid adder can enhance parallelism within systolicarrays, enabling the concurrent execution of multiple operations. This results in improved throughput, especially in applications demanding high-speed data processing.
- Potential Reduction in Power Consumption: Depending on thespecificimplementationandoptimizationstrategies,the hybrid adder offers a reduction in power consumptioncompared to traditional adder architectures.
- Thisadvantageiscrucialforenergy-efficientVLSIdesigns, particularly in battery-powered or low-power applications.

4. EXPERIMENTALANALYSIS

Figure 2 shows proposed simulation result for N=32. Here a &b are the inputs, P indicates the product of the inputs, N indicates the size of the bits.

Fig2:ProposedSimulationResultForN=32

Figure 3 shows the proposed area measurements for N=32. Here, 1790 numbers of LUT's are used out of available 134600 which consumes 1.33 of utilization. Here, 128 number of IO are usedout of available 500, which consumes 25.60 of utilization.

Resource	Estimation	Available	Utilization...
LUT	1790	134600	1.33
IO	128	500	25.60

Fig3:ProposedAreaForN=32

Proposed Power Measurements

Figure 4 shows proposed power measurement for N=32. Here,the total power is 123.260W, static power includes PL static is 1.235W,Dynamicpowerincludessignalis31.547W,Logicis 34.297 and I/Ois57.416W.Figure 5 showsProposedsetupdelay for N=32. Here Total Delay is 91.743, maximum Logic Delay is 17.214, maximum Net Delay is 74.529.Figure 6 shows Proposed HolddelayforN=32.HereTotalDelayis3.484,maximumLogic Delay is 1.832, maximum Net Delay is 1.651.

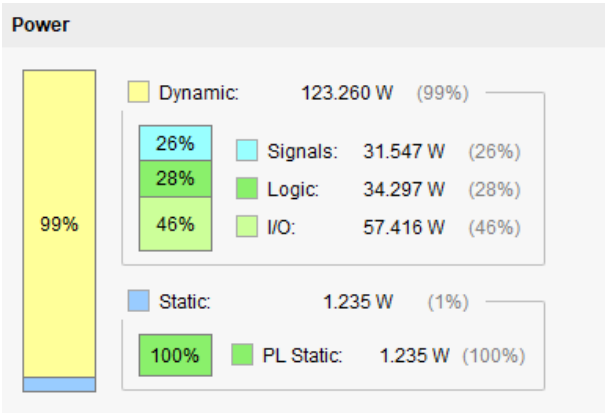

Fig4:Proposedpowerfor N=32

Fig5:ProposedsetupdelayforN=32.

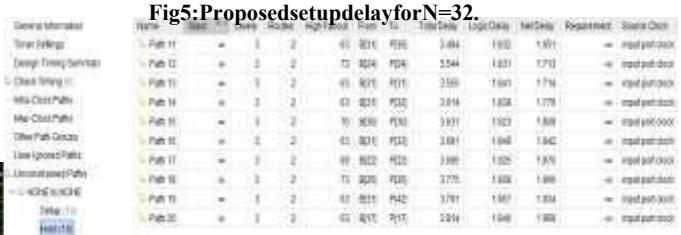

Figure6:ProposedHolddelayforN=32.

5. CONCLUSION

The major problems in existing multiplier designs, like Baurn and Wallace multipliers, include high power consumption, large chiparea,andsignificantpropagationdelays.Theseissuesareexacerbated by the increasing demand for higher computational speed and theneed for real-time processing in applications like image processingand machine learning. Furthermore, the lack of error detectionmechanisms in these systems can lead to inaccuracies, especially invariable operating conditions.

Additionally, the complexity of the circuitry in traditional designs limitsscalability,makingitdifficulttointegratethesemultipliersinto modern VLSI systems where space and power are premium. As aresult, there is aneedformore efficient architecturesthatcan address theseshortcomingswhileprovidinghigh-speedperformance,reduced power consumption, and reliability in various applications.

To address the limitations of existing multiplier architectures, we propose a systolic multiplier design that incorporates a hybrid multiplexer-dependent adder, systolic array, and Razor Flipflop for errorcorrection.Themultiplexer-dependentadder,consistingofafull adder and a 2-to-1 multiplexer, reduces the complexity of arithmetic operations, improving overall speed. The systolic array ensures parallelism, significantly enhancing processing speed by allowing simultaneous calculations. Finally, the Razor Flipflop introduceserror detection and correction capabilities, ensuring that the systemremains reliable under varying operating conditions. This designoffers a more efficient solution for high-speed, low-power multiplierapplications in VLSI systems.

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