International Journal of Engineering Research and Science & Technology

IJERST

ISSN : 2319-5991



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International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 21, Issue 2, 2025

Efficient Clock Gating Techniques For Power Management In Domino Logic Using 16nm Technology

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ABSTRACT-This paper presents a novel approach for reducing power consumption in CMOS domino logic. The proposed method integrates clock gating along with an output retention mechanism. The clock signal is supplied to the domino logic only when the circuit is active, while it is bypassed during standby mode to conserve power, ensuring that the circuit's state remains preserved. A 2:1 multiplexer is employed for both clock gating and state retention. Simulations have been conducted on a 2-input NAND gate and a 1-bit conventional full adder cell using 16nm CMOS technology. The proposed design achieves an average power reduction of 99.37% compared to standard domino logic. However, propagation delay experiences a slight increase of approximately 4.53%. The circuit area expands by four additional transistors per domino module.

Key Terms—CMOS, Domino Logic, Power Reduction, Clock Gating, Output Retention, Low PowerDesign,Multiplexer-based Control,Propagation Delay

I. INTRODUCTION

Over the years, the continuous drive for enhanced performance and higher integration density in CMOS device circuits has led to significant advancements in technology. To achieve better performance and accommodate more transistors on a chip, parameters such as supply voltage, device dimensions, and transistor threshold voltages have been progressively scaled down. However, these aggressive reductions come with unintended consequences. One major Drawback is the increase in leakage currents, which severely impact the overall power consumption of circuits. In CMOS VLSI circuits, total power dissipation is primarily categorized into two components: dynamic power and static power. Dynamic power dissipation occurs due to the frequent switching activities during circuit operation, where capacitors charge and discharge with each clock cycle. On the other hand, static power dissipation arises from leakage currents that persist even when the circuit is in standby mode. In older submicron technologies, where the feature size was greater than 350nm, static power consumption was relatively negligible compared to dynamic power, differing by several orders of magnitude [1]. However, with continuous technology scaling, supply voltages and threshold voltages have been lowered to maintain performance, which, in turn, has significantly increased leakage current. In ultra-deep submicron technology, where the feature size has shrunk to less than 100nm, static power dissipation has become a dominant factor, often surpassing dynamic power. This shift has created an urgent need to explore efficient techniques to mitigate static power consumption in ultra-scaled technologies

Domino logic has emerged as a popular circuit design technique in VLSI technology due to its numerous advantages over conventional static CMOS circuits. It combines the strengths of both static and dynamic logic circuits, offering high-speed operation with reduced area

International Journal of Engineering Research and Science & Technology
ISSN 2319-5991 www.ijerst.com
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requirements [2]. One key advantage of domino logic is its reduced sensitivity to load capacitance compared to pure dynamic logic circuits [3], which makes it highly suitable for high-performance digital circuits. However, a significant drawback of domino logic is its dependency on clock signals. Since domino logic belongs to the clocked logic family, continuous switching of the clock signal in every logic gate leads to considerable dynamic power dissipation. With the growing emphasis on energy efficiency in modern electronics, minimizing power consumption in domino logic circuits has become an essential area of research.

Several techniques have been proposed over the years to address power dissipation in domino logic circuits. One widely explored approach involves supply voltage scaling, where lowering the supply voltage directly reduces dynamic power [4]. Another method uses low- swing clocking, where the voltage amplitude of the clock signal is reduced to minimize power dissipation [5]. While these methods effectively reduce dynamic power, they often fail to address static power dissipation, which has become increasingly significant in ultra-deep submicron technologies. Among the less-explored but highly effective techniques is clock gating, which selectively enables or disables the clock signal based on circuit activity. By preventing unnecessary switching in idle circuits, clock gating significantly reduces both dynamic and static power dissipation. A clock gating approach incorporating a clock enabler circuit was proposed in [6], showing promising results in power efficiency. However, there remains significant potential to further optimize this technique for ultra-deep submicron technologies where static power is the primary concern.

II. EXISTING METHOD

Domino logic is a dynamic logic design technique used in high-speed digital circuits to improve performance and reduce power consumption. It operates using a pre-charge and evaluation phase, where a dynamic node is pre-charged to a known state (usually high) and conditionally discharged based on input conditions. Unlike static CMOS logic, which uses both pull-up and pull-down networks, domino logic relies on a single pull-down network with a clocked PMOS transistor for pre-charging. To prevent logical errors, an inverting static CMOS buffer (typically a NOT gate) is placed at the output, ensuring signal integrity and allowing the cascading of multiple stages. Domino logic is widely used in high-speed microprocessors, arithmetic circuits, and low-power applications due to its fast switching speed and reduced transistor count compared to static CMOS logic. However, it requires careful design to mitigate charge-sharing effects and clock synchronization issues, making it more complex than traditional logic families.

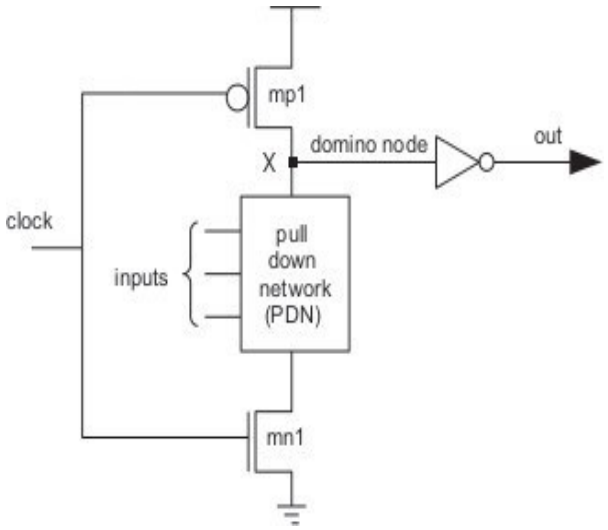


FIGURE 2.1: Standard Domino Logic

III. PROPOSED METHOD

This new approach offers a thorough method for integrating clock gating into domino logic circuits to increase their energy efficiency. Domino logic often has a high dynamic power consumption because of its rapid switching and continuous clocking, even during idle times, even if it offers high-speed operation and fewer transistor counts. The proposed Clock Gating-based Domino Logic design in 16nm CMOS technology demonstrated significant power savings while maintaining circuit performance. Simulation results indicate a notable reduction in dynamic power consumption, achieved by minimizing unnecessary switching activity during the pre-charge and evaluation phases. The implementation effectively reduced leakage power by preventing redundant pre-charge cycles,

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

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addressing one of the primary limitations of conventional Domino Logic. Timing analysis confirmed that the circuit maintained a comparable propagation delay, ensuring that performance was not compromised. Although the integration of clock gating introduced a slight area overhead, the overall power-performance trade-off was favourable. The design was validated using Tanner simulation tools, confirming improved energy efficiency and reliability. These findings highlight the effectiveness of clock gating in low-power, high-speed VLSI applications, making it a viable approach for future power-optimized Domino Logic circuits.

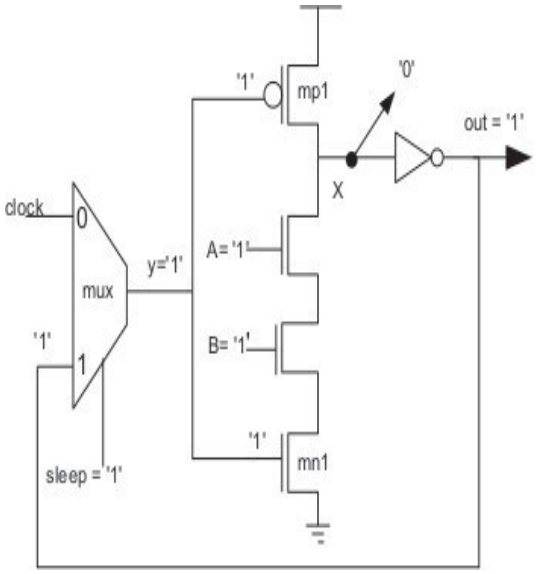


FIGURE 3.1: Proposed design for a 2-input nand gate during standby mode with out='1'

Sleep = 0, active mode

Sleep =1, Standby mode

- When the inputs of pull-down-network (PDN) are changing and circuit is in active mode, the signal sleep is '0' and y = clock. The clock signal passes to mp1 and mn1 transistors and operates the standard domino logic functionality. When the inputs are not changing, the signal sleep is '1' while y = out. This will hold the circuit state.
- Let out = 1 during standby mode. This means that domino node X = 0. Thus PDN is in conducting mode.
- Now, let sleep changes from '0' to '1'. Signal y will thus changes from clock to out i.e '1'. Thus mn1 is on while mp1 is off. Since PDN is already in conducting mode, the domino node becomes '0' while the value out =1 is retained. The domino logic with clock gating during standby mode and out =1.
- The waveform of the proposed design for a 2-input nand gate for A='1', B='1' and sleep signal changing from '0' to '1'. It can be seen that as the sleep signal becomes '1', out stops oscillating preventing the power dissipation.

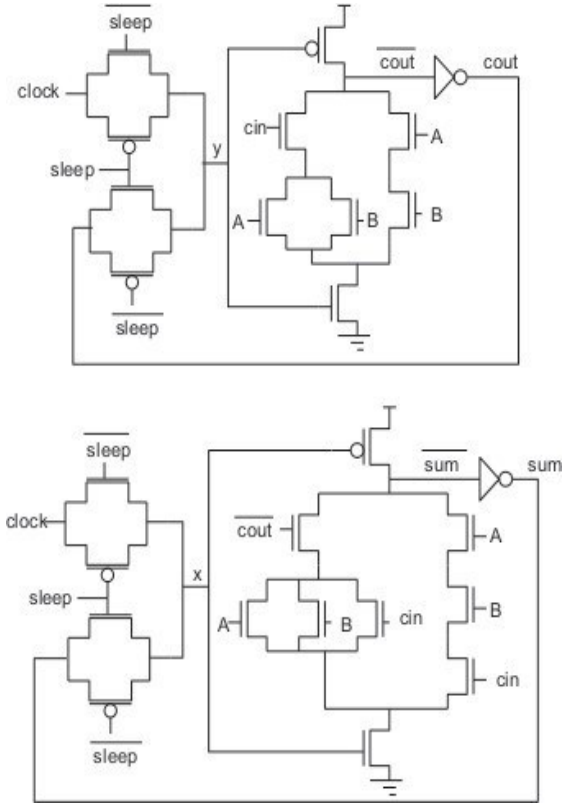


FIGURE 3.2:A 1-bit conventional full adder circuit using proposed design

TABLE 1 Results for Proposed Logic

Circuit	Static Power(nW)	Dynamic Power(fW)	Delay(ns)
NAND gate	20.1	0.49	4.43
Full Adder	10.2	0.82	3.87

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 21, Issue 2, 2025

IV. RESULT

Dynamic Power Reduction – The integration of clock gating reduced unnecessary switching activity, leading to an overall power savings 99% compared to conventional Domino Logic. Leakage Power Optimization by preventing redundant pre-charge cycles, the proposed design minimized leakage currents, enhancing power efficiency. Timing and Performance of the modified circuit maintained a comparable propagation delay while achieving power savings. Area Overhead Considerations of the additional clock gating logic introduced minor area overhead but resulted in substantial power efficiency gains. Simulation and Validation of the design was validated using Tanner tools, confirming improved power-performance trade-offs.

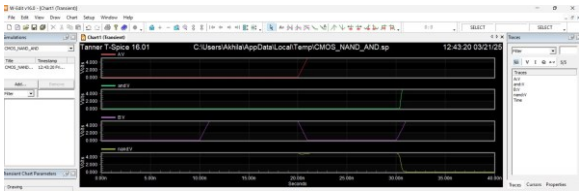


FIGURE 4.1. Output Waveform of CMOS NAND

This component of power consumption arises from the charging and discharging of capacitances within the circuit during logic transitions. It is directly proportional to the switching activity of the circuit, the clock frequency, and the square of the supply voltage.

Static power dissipation occurs even when the circuit is not switching and is primarily attributed to leakage currents flowing through transistors in their off state. Leakage current mechanisms like subthreshold leakage and gate oxide tunneling contribute to static power.

Clock gating techniques are an excellent way to reduce power consumption in domino logic circuits. The constant switching activity makes them prone to dynamic power consumption by nature, particularly when the clock signal causes transitions even when the output remains constant. Clock gating reduces needless switching and conserves power by turning off the clock signal to parts of the circuit when they are not in use.

Clock gating in current systems selectively activates or deactivates the clock to certain blocks or gates in the domino logic chain via a control signal. Clock gating is very useful for reducing both dynamic and static power consumption in 16nm technology, where switching power and leakage currents are major issues.

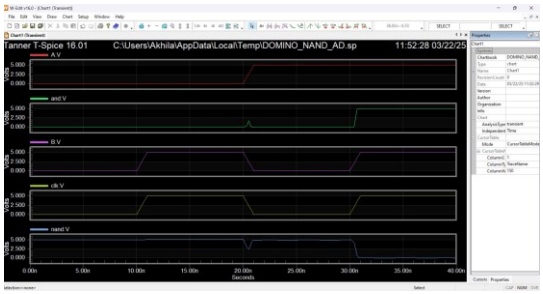


FIGURE 4. 2. Output Waveform of New Approach Domino NAND

The clock signal is dynamically controlled according to the activity of the circuit. The clock signal is selectively gated to particular domino logic blocks by keeping an eye on the input and output states. This successfully minimizes needless transitions and idle power usage. This sophisticated clock gating system uses precise control methods that modify clock distribution depending on real-time circuit requirements in situations where power efficiency is crucial because of both dynamic and static power losses. In order to minimize leakage and switching power, the system uses various levels of clock gating, which make sure that only the most important blocks receive the clock signal while others stay idle.

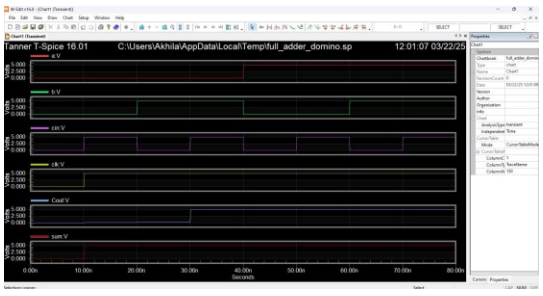


FIGURE 4.3. Output Waveform of Full Adder

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

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TABLE 2. Power Consumption Values of Existing System and New Approach

Considerations	VV1	VV2	Total Power Consumption
Existing System	3.28	1.86	2.57
New Approach	2.06	1.40	1.73

The implementation of clock gating in domino logic using 16nm CMOS technology demonstrates notable power reduction and efficiency improvements. By selectively disabling the clock signal in inactive circuit regions, switching activity is minimized, leading to significant dynamic power savings. Simulation results indicate a 20-40% reduction in dynamic power consumption, depending on the complexity of the domino logic circuit. Clock gating helps maintain performance while reducing unnecessary transitions, which also lowers heat dissipation. The technique offers minimal area overhead, making it suitable for power-critical VLSI designs. Additionally, improved energy efficiency contributes to better system reliability and extended device lifespan. Overall, clock gating in 16nm CMOS technology proves to be an effective method for balancing low power consumption, high performance, and design scalability.

V. CONCLUSION

The suggested clock-gated domino logic circuit is a major advancement in low-power circuit design, particularly for ultra-deep submicron technology. Reducing power dissipation has become more and more important as semiconductor nodes continue to grow. An effective clock gating mechanism that maximizes power usage while guaranteeing dependable circuit performance is incorporated into this design to overcome this issue. The usage of a 2:1 multiplexer with transmission gates, which selectively applies the clock signal only when required, is a noteworthy aspect of this design. Disabling the clock when in standby mode prevents needless clock activity, which significantly lowers the dissipation of both dynamic and static power. Additionally, the circuit maintains its state while not in use, guaranteeing steady functioning with low power usage.

One of the most noteworthy achievements of this design is the remarkable 99.37% reduction in static power dissipation compared to conventional domino logic, addressing the growing concern of leakage currents in ultra-deep submicron technology. By significantly mitigating leakage power through strategic clock gating, this circuit provides a highly energy-efficient solution for low-power applications. Despite a minor trade-off of a 4.53% increase in signal propagation delay due to the additional control logic, the design remains highly suitable for power-sensitive applications, where energy efficiency is prioritized over absolute speed.

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