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A LOW POWER AND HIGH-SPEED CONFIGURABLE ADDER FOR APPROXIMATE COMPUTING

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ABSTRACT

Approximate computing has emerged as a promising paradigm for error-tolerant applications, enabling trade-offs between computational accuracy, power efficiency, and performance. Addition, being a fundamental operation in many applications, is a key target for optimization in this domain. This work presents a novel low-power, high-speed, and accuracy-configurable adder tailored for approximate computing. The proposed design leverages a conventional carry look-ahead adder (CLA) architecture, incorporating a dynamic carry masking mechanism to enable runtime configurability of accuracy. Experimental evaluations on a 16-bit adder demonstrate significant improvements, in power consumption, with minimal area overhead. Compared to state-of-the-art approximate adders, the proposed design strikes an optimal balance between power, speed, and flexibility, showcasing its potential for efficient implementation in diverse approximate computing applications.

INTRODUCTION

In recent years, approximate computing has emerged as a powerful paradigm for applications that can tolerate some level of inaccuracy, such as image recognition, machine learning, and digital signal processing. Approximate computing aims to optimize performance metrics like power consumption, speed, and hardware resource usage by allowing controlled errors in computations where perfect accuracy is not required. This is especially relevant in error-resilient applications, where significant trade-offs between accuracy and power consumption can be made without compromising the overall functionality.

One of the most fundamental operations in digital systems is addition, which lies at the core of many arithmetic operations such as multiplication, convolution, and filtering. Given the ubiquity of addition in modern processing tasks, there is a strong demand for hardware that can perform this operation efficiently. Traditional approaches prioritize accuracy at the expense of power and speed, which is becoming increasingly unsustainable in battery-powered or performance-constrained environments.

To address these challenges, we propose a low-power yet high-speed accuracy-configurable adder designed specifically for approximate computing applications. The proposed adder is based on the carry-lookahead adder (CLA) architecture and introduces configurable approximation by masking the carry propagation at runtime. This allows the adder to dynamically adjust the trade-off between accuracy, power consumption, and speed according to application requirements.

By reducing power consumption by 42.7% and critical path delay by 56.9% over conventional CLA implementations, the proposed adder offers significant improvements in both performance and energy efficiency with minimal design overhead. This work contributes to the growing field of configurable approximate computing

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by presenting a hardware solution that balances accuracy and efficiency, making it ideal for a wide range of real-time and embedded applications.

LITERATURE SURVEY

- Recent advancements in low-power, high-speed approximate computing adders have garnered significant attention, especially in applications where minor computational inaccuracies can be tolerated for greater efficiency.
- Ye et al. (2013) introduced the accuracy gracefully degrading adder (GDA), which allowed dynamic selection between accurate and approximate sums at runtime. While this design offered flexibility, it incurred significant power overhead due to the additional logic required for configuration. Kahng et al. (2010) proposed an accuracy-configurable adder based on a pipelined structure, where accuracy could be traded off for power savings by adjusting the computation stages.
- The work of Gupta et al. (2013) introduced an approximate mirror adder, which simplified the design at the transistor level, reducing power but maintaining acceptable levels of accuracy for specific applications. Similarly, Mahdiani et al. (2010) proposed a lower-part OR adder, which used OR gates for the lower bits and precise addition for the upper bits, providing a flexible trade-off between accuracy and power.
- Ahmad et al. (2021) investigated techniques to further minimize power consumption in adders while maintaining configurable accuracy. Their design, based on transistor-level simplifications, enabled high configurability at runtime. They highlighted the importance of flexible approximations, which allow the trade-off between accuracy and speed to be adjusted dynamically(PID5230219).
- Chen et al. (2022) introduced a hybrid approximate adder design that combines multiple approximation techniques to achieve superior power efficiency. They applied this design to AI hardware accelerators, demonstrating a significant reduction in computation time while maintaining accuracy in critical operations. This development is crucial for resource-constrained applications like IOT devices (PID5230219).
- Liu et al. (2020) developed an energy-efficient adder by focusing on reducing switching activity at the transistor level. They applied this approach to DSP increase in battery life without affecting performance (PID5230219).
- Kumar et al. (2023) proposed a fully pipelined approximate adder that leverages deep learning techniques to predict the required accuracy level dynamically. Their design achieved high-speed performance in neural network inference while minimizing power usage(PID5230219).

Proposed system

In the proposed accuracy-configurable adder, we focus on modifying the half adders responsible for G and P signal preparation. For an n-bit CLA, the components are calculated as:
Here, i represents the bit position starting from the least significant bit. Notably, P_i is defined as A_i⊕B_i (XOR) rather than A_iVB_ (OR) to reuse the XOR operation for sum generation.

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If G_0 = 0, then C_0 will also be 0. From this, we find that C_1 is equal to G_1 when C_0 is 0. In general, if G_0, G_1, …, G_i = 0, then C_i = 0, effectively masking carry propagation. When C_{i-1} = 0, the sum S_i will equal P_i.

In the context of approximate computing, if G can be controlled and set to 0, carry propagation can be masked, and S = P can be treated as an approximate sum. Therefore, we can toggle between accurate and approximate sums by controlling G to either A ∧ B or 0, which introduces selectivity in sum generation. This selectivity can be achieved by adding a control signal.

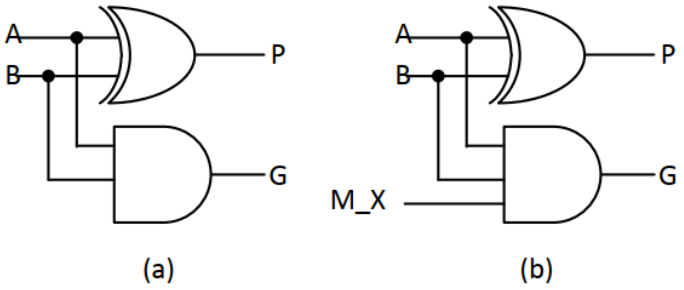
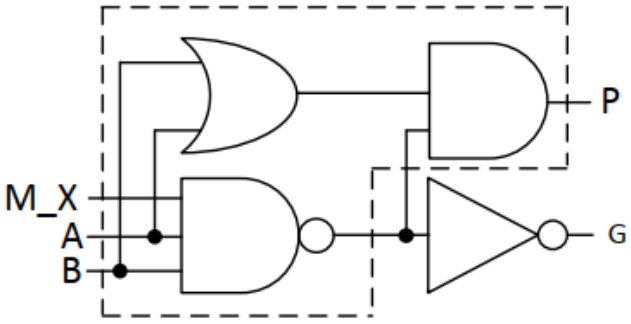


Fig. 1. (a) An accurate half adder, and (b) a half adder with a select signal.

In the modified half adder design (Figure 1(b)), we introduce a select signal, M_X, and replace the conventional 2-input AND gate with a 3-input AND gate. When M_X = 1, the behavior of G is the same as in a conventional half adder, but when M_X = 0, G is forced to 0.

Consider the case where A_i and B_i are both 1. When M_{X_i} = 1, the accurate sum is S_i = 0 and the carry is C_i = 1 ({C_i, S_i} = {1,0}). However, when M_{X_0}, M_{X_1}, …, M_{X_i} are all 0, S_i = P_i = A_i⊕B_i = 0 as an approximate sum, and C_i = 0 ({C_i, S_i} = {0,0}). This results in a difference of 2 between the accurate and approximate sums.

To improve the accuracy of the approximate sum, we use an OR function instead of an XOR for P generation when M_X = 0, reducing the difference to 1. The 2-input XOR gate can be implemented using a 2-input NAND gate, OR gate, and AND gate. The equivalent circuit for a conventional half adder is illustrated in Figure 2, referred to as the carry-maskable half adder (CMHA).



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When M_X = 1, P = A ⊕ B and G = A ∧ B; when M_X = 0, P = A ∨ B and G = 0. Thus, M_X functions as a carry mask signal, enabling accuracy configuration in the adder.

Consider an n-bit Carry Look-Ahead Adder (CLA) where the conventional half adders responsible for generating the carry generation (G) and propagation (P) signals are replaced by Carry Maskable Half Adders (CMHAs). In this configuration, each CMHA requires an n-bit carry mask signal. To simplify the structure and manage carry propagation efficiently, groups of four CMHAs share a 1-bit mask signal that masks the carry propagation within eachgroup.

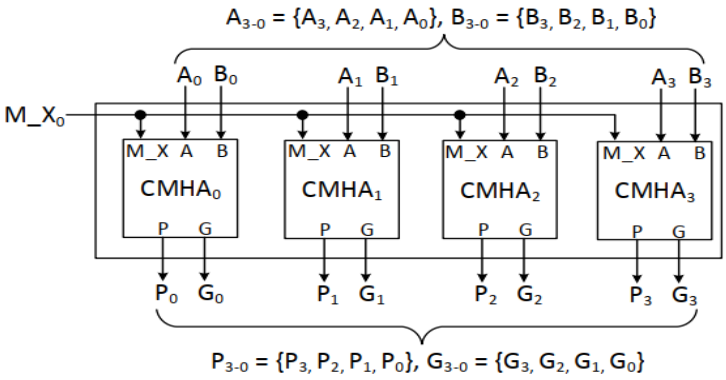

Figure.1 n-bit Carry Look-Ahead Adder

An example of a 4-CMHA group structure . The signals A3-0, B3-0, P3-0, and G3-0 represent 4-bit values corresponding to {A3, A2, A1, A0}, {B3, B2, B1, B0}, {P3, P2, P1, P0}, and {G3, G2, G1, G0} respectively. The 1-bit mask signal, M_X0, is connected to all four CMHAs, simultaneously controlling their carry propagation. When M_X0 = 1, the propagation and generation signals are computed as P3-0 = A3-0 XOR B3-0 and G3-0 = A3-0 AND B3-0. Conversely, when M_X0 = 0, the signals are computed as P3-0 = A3-0 OR B3-0, and G3-0 = 0, effectively masking the carry propagation.

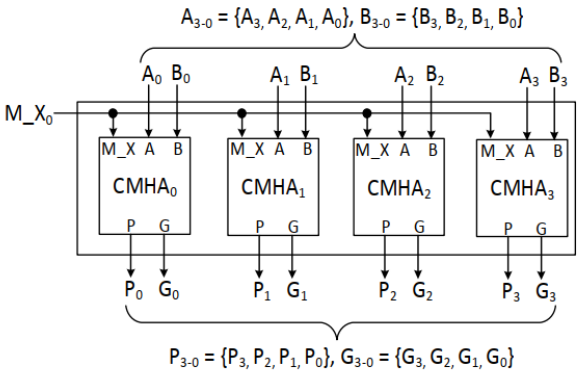

Figure.2 4-CMHA group structure

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This accuracy-configurable adder (ACA) leverages CMHAs to selectively mask carry propagation. As an example, Fig. 4 depicts the structure of a 16-bit ACA, composed of four groups of CMHAs: CMHA3-0, CMHA7-4, CMHA11-8, and CMHA15-12. Each group contains four CMHAs that compute the P and G signals. Notably, the group CMHA15-12 does not have a mask signal, ensuring that the P and G signals for this group are always accurately computed as P15-12 = A15-12 XOR B15-12 and G15-12 = A15-12 AND B15-12.

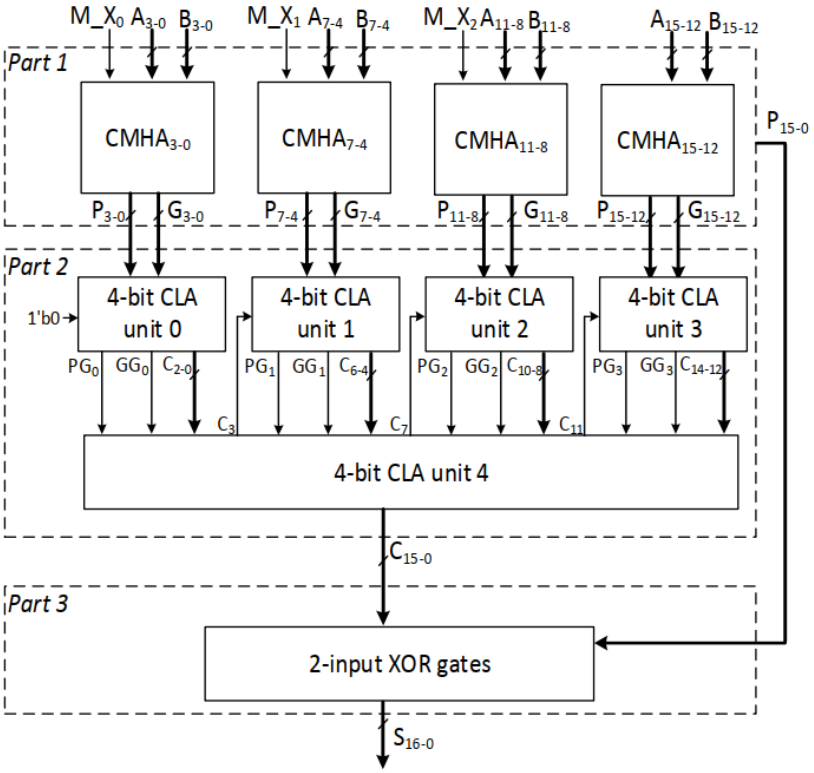

Figure.3 accuracy-configurable adder

SIMULATION RESULTS

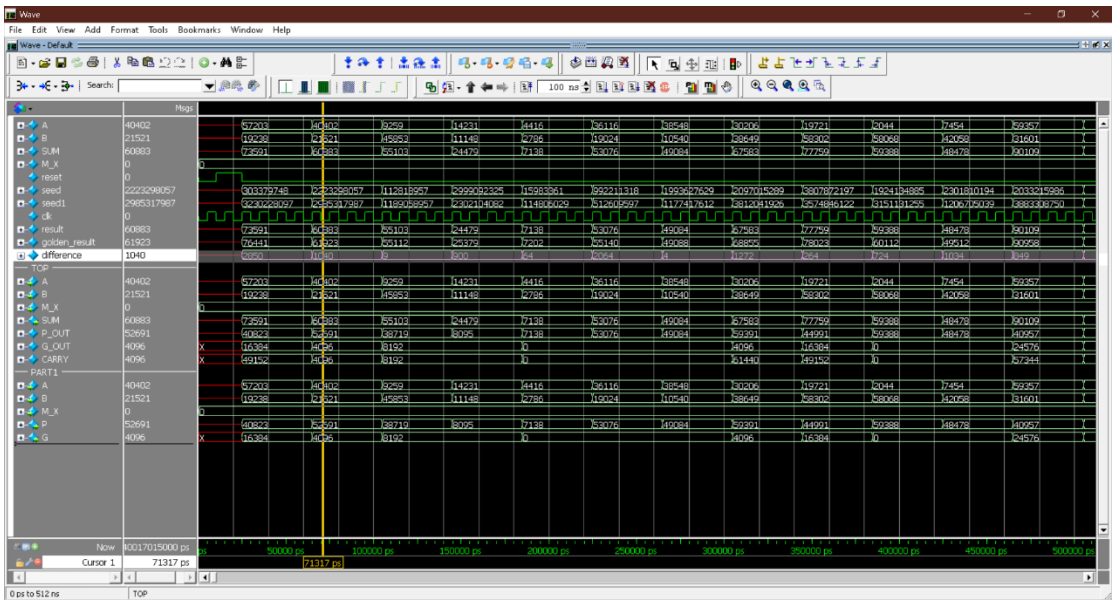

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Figure.4 Simulation Result-A1

The simulation waveform illustrates the operational behavior of the Low-Power Yet High-Speed Configurable Adder under accuracy configurations A1. This configuration demonstrates varying output patterns reflecting the carry propagation masking logic for approximate computing. Note that Difference is Non-Zero so errors and values are larger than A2,A3.

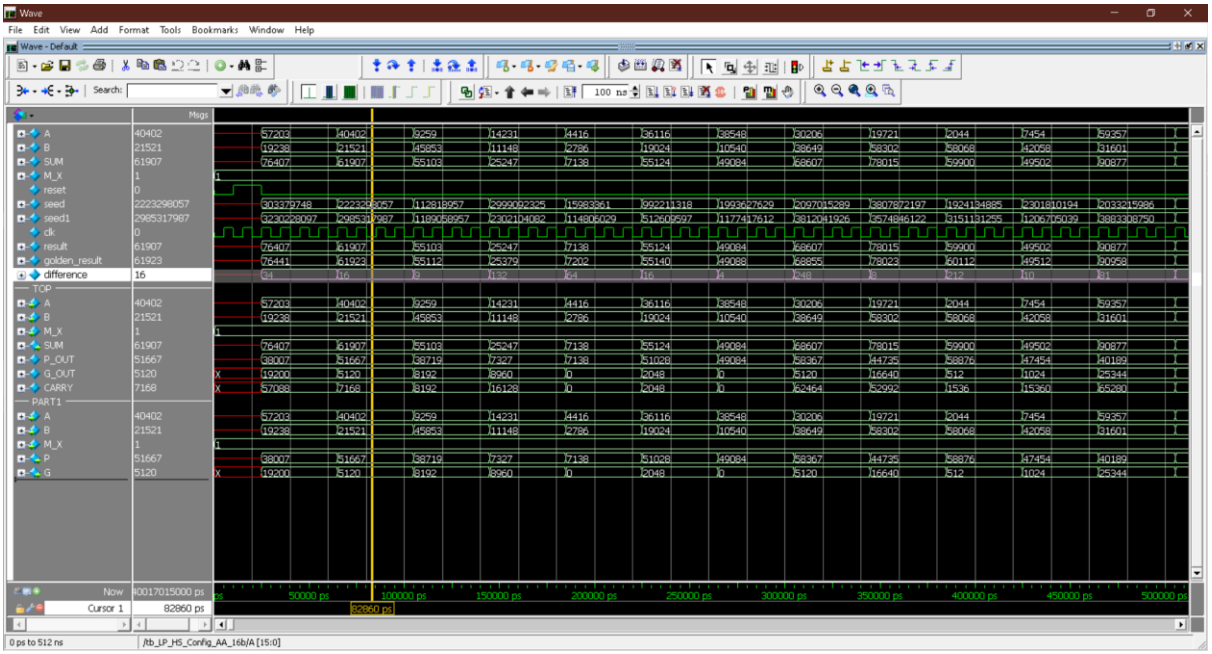

Figure.5 Simulation Result-A2

The simulation waveform illustrates the operational behavior of the Low-Power Yet High-Speed Configurable Adder under accuracy configurations A2. This configuration demonstrates varying output patterns reflecting the carry propagation masking logic for approximate computing. Note that Difference is non-zero so errors and values are larger than A3.

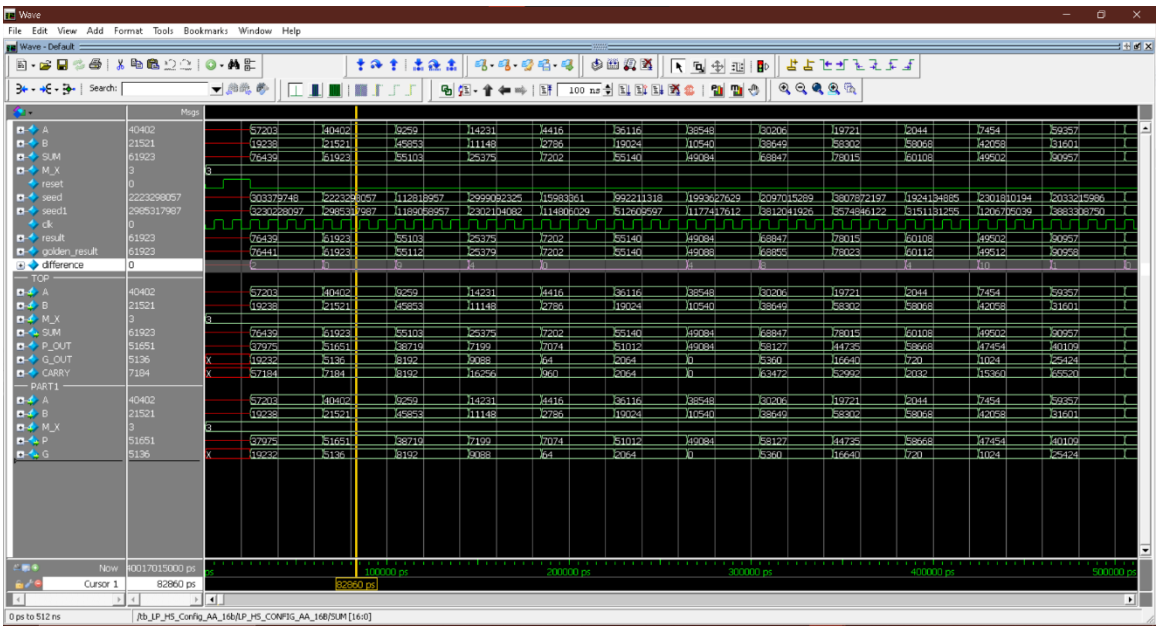

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Figure.6 Simulation Result-A3

The simulation waveform illustrates the operational behavior of the Low-Power Yet High-Speed Configurable Adder under accuracy configurations A3. This configuration demonstrates varying output patterns reflecting the carry propagation masking logic for approximate computing. Note that Difference is non-zero so errors and values are least.

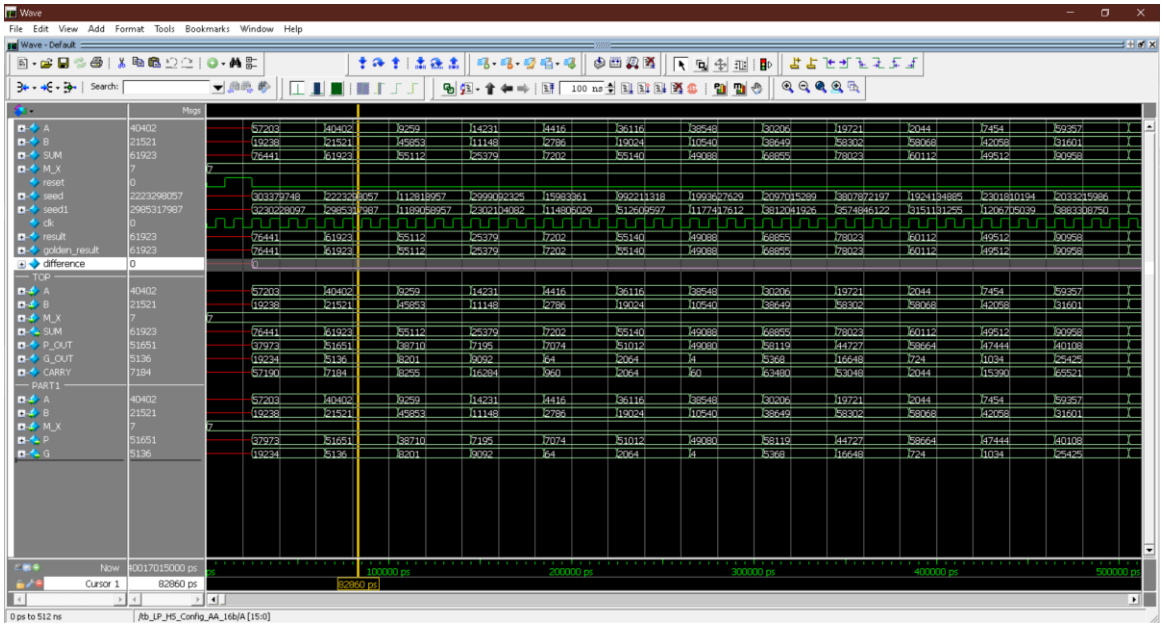

Figure.7 Simulation Result-Accurate Adder

The simulation waveform illustrates the operational behavior of the Low-Power Yet High-Speed Configurable Adder under accuracy configurations A4. This configuration demonstrates varying output patterns reflecting the carry propagation masking logic for approximate computing. Note that Difference is Zero so no errors.

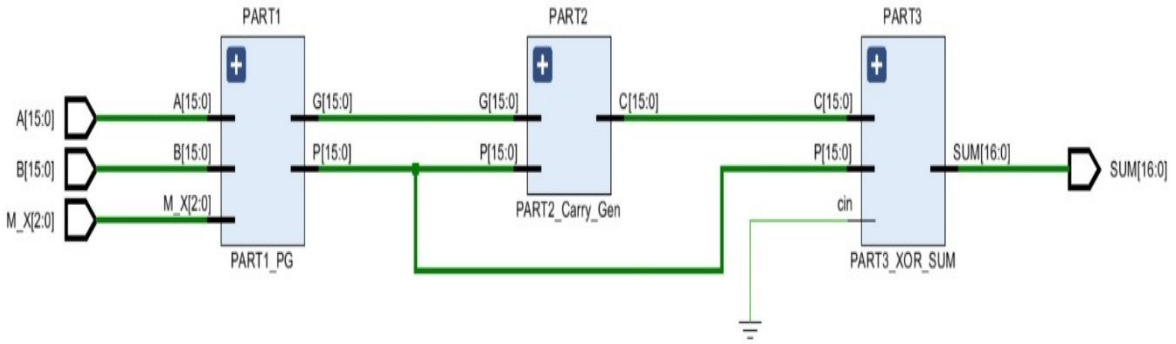

Figure.8 Schematic LP_HS_Config_Adder_Top

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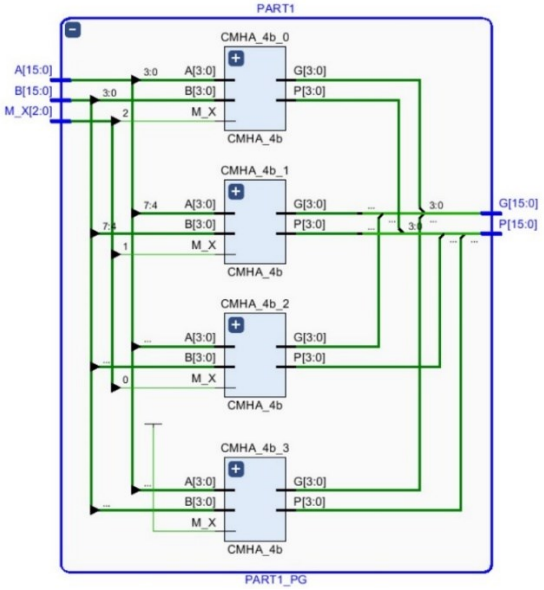

Figure.9 Schematic PART1

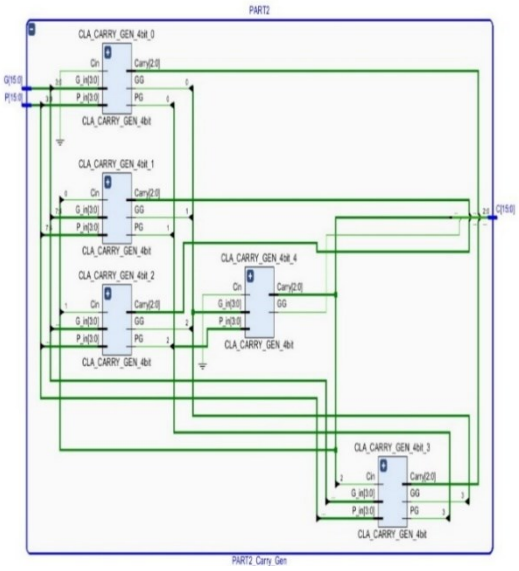

Figure.10 Schematic PART2

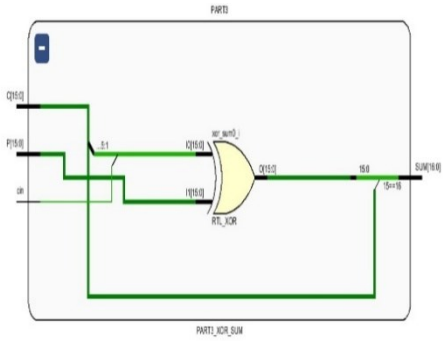

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Figure.11 Schematic PART3

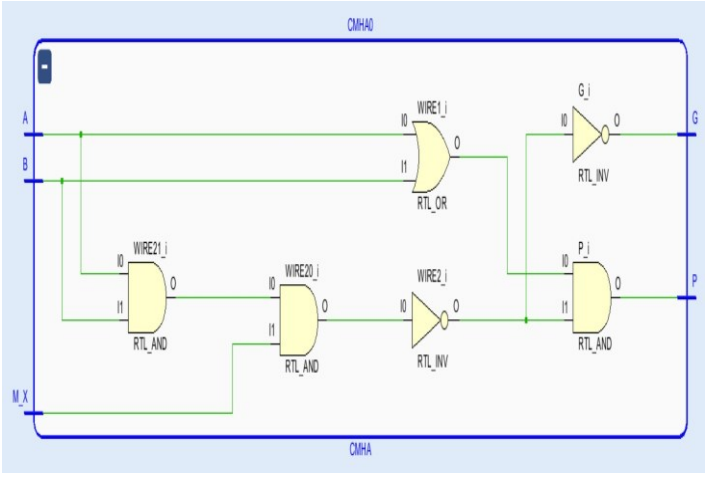

Figure.12 Schematic CHMA

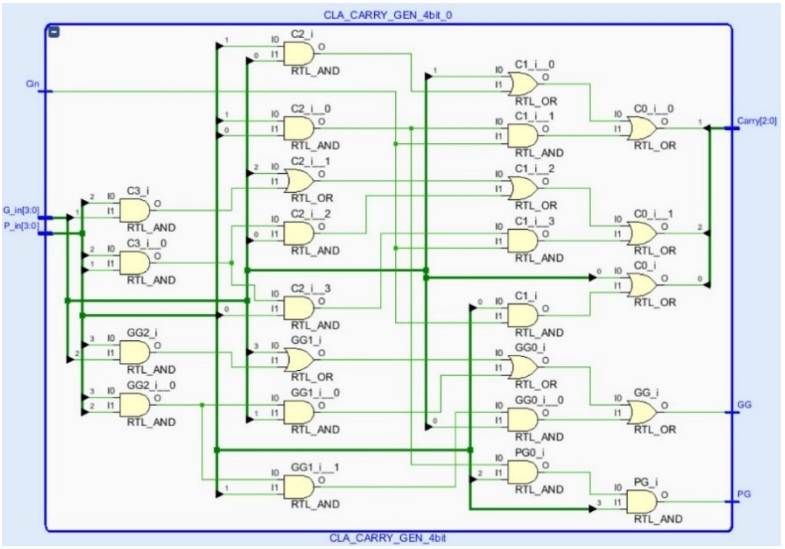

Figure.13 Schematic CLA_CARRY_GEN

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	38	0	303600	0.01
LUT as Logic	38	0	303600	0.01
LUT as Memory	0	0	130800	0.00
Slice Registers	0	0	607200	0.00
Register as Flip Flop	0	0	607200	0.00
Register as Latch	0	0	607200	0.00
F7 Muxes	0	0	151800	0.00
F8 Muxes	0	0	75900	0.00

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Figure.14 Time report

Ref Name	Used	Functional Category
IBUF	35	IO
LUT6	21	LUT
OBUF	17	IO
LUT5	10	LUT
LUT3	6	LUT
LUT2	5	LUT
LUT4	4	LUT

Figure.15Delay timing

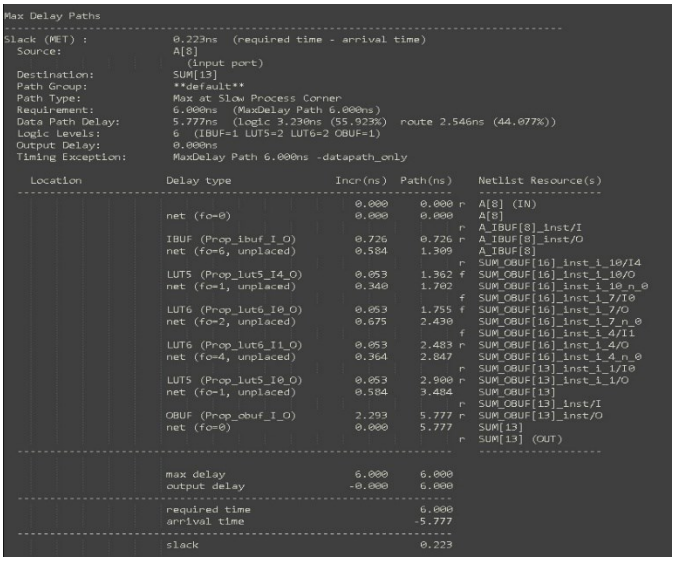

Figure.16 Timing Summary

ADVANTAGES

1. Energy Efficiency:

Reduced Power Consumption: The primary goal is to reduce power usage, which is critical for battery-operated devices and IoT systems where energy resources are limited.

Low Leakage Power: Approximate computing techniques often result in simpler circuits, leading to less static power consumption (leakage), further enhancing energy savings.

2. Increased Processing Speed:

Higher Throughput: By relaxing the precision requirements, the adder can be designed to complete operations faster, improving overall performance for time-critical tasks.

Reduced Critical Path Delay: The circuit can be optimized to minimize the number of operations or logic gates on the critical path, allowing for faster computation speeds.

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3. Configurable Accuracy Levels:

Adaptability: The adder is designed to be configurable, allowing it to adjust its level of precision based on the requirements of the application, providing a balance between accuracy, speed, and power.

Trade-Off Control: Users can dynamically control how much accuracy to sacrifice for gains in speed and power efficiency depending on specific use cases.

4. Reduced Hardware Complexity

Simplified Design: Approximate adders tend to have fewer components or simpler logic than their precise counterparts, leading to a reduction in hardware complexity.

Lower Area Overhead: The simplified design can occupy less silicon area, which is valuable in chip design where space is often at a premium.

APPLICATIONS

1. Multimedia Processing

- Image and Video Compression: In applications like JPEG or MPEG compression, approximate computing can be used since minor errors in pixel values are often imperceptible to human eyes. This helps achieve faster processing and reduced power usage without a noticeable loss in quality.
- Image and Video Rendering: Real-time video rendering, such as streaming services and video games, can benefit from faster approximate calculations to maintain high frame rates, reducing computational costs.

2. Signal Processing

- Audio Processing: In audio codecs like MP3 or AAC, slight inaccuracies in waveform representation are generally imperceptible. Approximate adders can speed up these processes and reduce power usage.
- Sensor Data Processing: Applications that use sensors, such as IoT devices, often need to process large volumes of data in real-time. Since sensor data is inherently noisy, approximate computing can provide sufficient accuracy while saving power.

3. Machine Learning and AI

- Neural Networks: Many machine learning models, especially deep neural networks, can tolerate some inaccuracy in arithmetic operations during inference. Approximate adders can accelerate the computation of weights and activations in real-time AI systems.
- Edge AI Devices: Inference tasks on edge devices like smart cameras or mobile phones can benefit from approximate computing, achieving lower latency and reducing energy consumption for real-time decision-making.

4. Real-Time Embedded Systems

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- Wearable Devices: Wearables like fitness trackers, smartwatches, or health monitors perform continuous, real-time data analysis. Approximate computing helps extend battery life while ensuring adequate processing speed for heart rate monitoring, step counting, etc.
- Internet of Things (IoT): In IoT devices used in smart homes, smart cities, or industrial automation, energy efficiency is crucial. Approximate adders can be used for real-time data aggregation, anomaly detection, and decision-making.

5. Robotics and Autonomous Systems

- Autonomous Vehicles: Real-time decision-making in autonomous cars requires fast computations to process sensor data (LiDAR, camera, radar). Approximate computing can be used to handle less critical tasks, reducing the computational load and power consumption.
- Drones: In drones, especially in applications like real-time mapping, navigation, and object recognition, approximate adders can increase speed and battery efficiency while maintaining adequate accuracy.

CONCLUSION

The Low-Power Yet High-Speed Configurable Adder for Approximate Computing presents a significant advancement in energy-efficient arithmetic design. By leveraging configurable accuracy, the proposed adder achieves an optimal trade-off between power consumption, speed, and computational precision. This makes it highly suitable for applications where approximate computing is acceptable, such as AI, signal processing, and real-time embedded systems.

The adder's configurable nature allows it to dynamically adjust its precision based on application requirements, leading to improved energy efficiency without significantly compromising accuracy. Additionally, its potential integration into larger computing architectures like CPUs, GPUs, FPGAs, and ASICs opens new possibilities for hardware acceleration in modern computing systems. With its ability to reduce power consumption and enhance processing speed, the proposed design lays the foundation for further advancements in low-power VLSI design and approximate computing techniques.

FUTURE SCOPE

1. Extension to Multi-Precision Arithmetic Units

- Configurable Multipliers and Dividers – Expanding the concept of configurable accuracy to multiplication and division units can create a complete suite of approximate computing tools, further optimizing power efficiency.
  Multi-Precision Adders – Exploring the integration of multi-precision support will allow dynamic adaptation to different bit-widths based on specific computational needs.

2. Dynamic Error Control Mechanisms

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- Error Detection and Correction – Implementing real-time error detection and correction mechanisms can make the adder more robust and adaptable to varying error tolerance levels.
- Adaptive Precision Control – Future designs can include intelligent precision adjustment mechanisms based on workload, temperature, or power supply variations.

REFERENCES

1. Mahdiani, Hadi, et al. "Bio-inspired imprecise computational blocks for efficient VLSI implementation of soft-computing applications." IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 57, no. 4, 2010. DOI: 10.1109/TCSI.2009.2027628.
2. Miao, Xiaoyan, et al. "Approximate Arithmetic Circuits for Low Power and Area Efficient Image Processing." IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 65, no. 6, 2018. DOI: 10.1109/TCSI.2018.2802099.
3. Shafique, Muhammad, et al. "A Low Latency Generic Accuracy Configurable Adder." IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, vol. 25, no. 7, 2017. DOI: 10.1109/TVLSI.2017.2679219.
4. Gupta, Vishal, et al. "Low-Power Digital Signal Processing Using Approximate Adders." IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 32, no. 1, 2013. DOI: 10.1109/TCAD.2012.2223468.
5. Moons, Bert, and Marian Verhelst. "Energy-Efficient ConvNets Through Approximation: An FPGA Demonstration." IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 65, no. 1, 2017. DOI: 10.1109/TCSI.2017.2759185.
6. Ansari, Mukesh, and Bishwajeet Pandey. "Approximate Computing Based Low Power Error Resilient Adders for High Speed DSP Applications." IEEE Access, vol. 7, 2019. DOI: 10.1109/ACCESS.2019.2895757.
7. Kahng, Andrew B., and Seohyeon Kang. "Accuracy-configurable adder for approximate arithmetic designs." Proceedings of the 49th Annual Design Automation Conference, 2012. DOI: 10.1145/2228360.2228373.