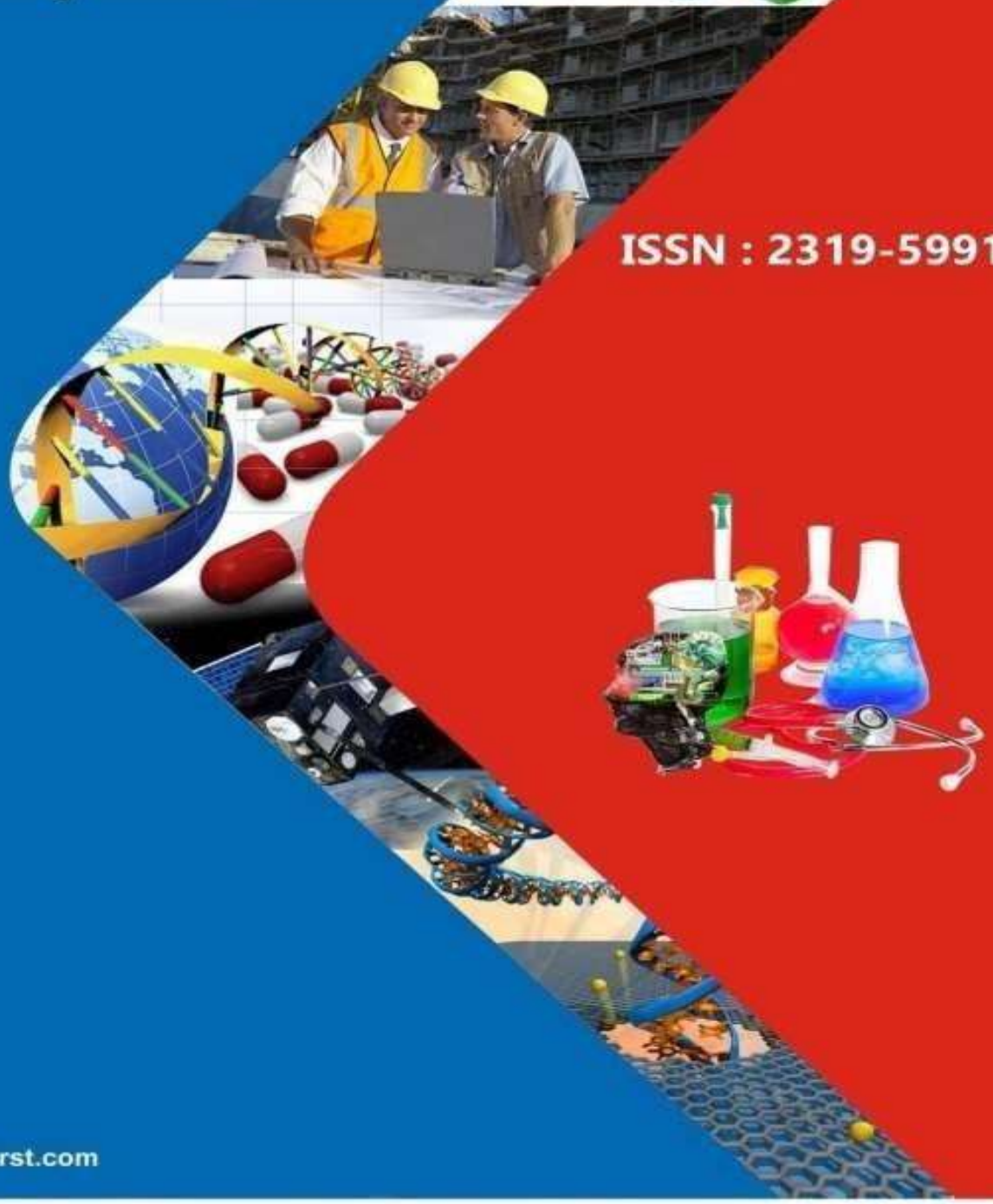
International Journal of Engineering Research and Science & Technology

IJERST

ISSN : 2319-5991



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International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 21, Issue 1, 2025

ANALYSIS OF VARIOUS APPROXIMATE ADDERS IN RIPPLE CARRY ADDER DESIGN

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ABSTRACT

This paper explores the implementation of various types of approximate full adders in Ripple Carry Adders (RCA) 4-bit configurations. These approximate adders are integrated at different bit positions within the RCA and evaluated based on multiple performance parameters. Approximate circuits are designed to simplify hardware complexity and enhance computational efficiency. In applications such as multimedia processing, where minor inaccuracies are acceptable, exact results are not always necessary, making approximate adders a viable alternative. This study compares different approximate full adders (AA0 to AA6) in terms of error percentage and overall performance, providing insights into their effectiveness in practical applications.

INTRODUCTION

Adders are one of the most essential components in digital circuits, widely used in applications such as digital signal processing, multimedia, and computer arithmetic. The Ripple Carry Adder (RCA) is a fundamental adder architecture known for its simple design and ease of implementation. However, it suffers from high propagation delay, as each carry bit must be computed sequentially. This delay becomes a critical bottleneck in high-speed computing applications. To address this challenge, researchers have explored approximate computing techniques, which offer a balance between accuracy and efficiency.

Approximate adders are designed by modifying conventional full adder circuits to reduce power consumption, delay, and hardware complexity. These adders introduce a small amount of computational error, which is tolerable in applications such as image/video processing, deep learning, and computer vision, where minor inaccuracies do not significantly affect overall performance.

This project analyses various approximate full adders by integrating them into different bit positions of 4-bit and 8-bit Ripple Carry Adders (RCA). The designs examined include NAND-based approximate adders, carry-based adders, and majority logic-based adders, each optimized for different performance metrics. The effectiveness of these approximate adders is evaluated in terms of power efficiency, area reduction, and error metrics such as Mean Error Distance (MED) and Normalized MED (NMED).

By systematically replacing conventional adders with approximate counterparts, the project aims to identify the most efficient configurations that enhance performance while keeping error rates within acceptable limits. The results of this study can be extended to higher-bit adders and complex arithmetic circuits, making significant contributions to low-power VLSI design.

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Ultimately, this research demonstrates how approximate adders can improve computational efficiency in modern digital systems, paving the way for more power-efficient and high-performance architectures in future computing applications.

Literature survey

1. Approximate Computing in Adders

V. K. Chippa et al. (2013) analyzed the concept of approximate computing and its application in arithmetic circuits, demonstrating how error-tolerant designs can enhance power efficiency in image processing and deep learning applications【1】. J. Schlachter et al. (2017) proposed a method for gate-level pruning, significantly reducing power consumption in adders

2. Approximate Ripple Carry Adders (RCA)

Ripple Carry Adders (RCAs) suffer from high propagation delay due to sequential carry computation. To address this, researchers have proposed approximate full adder designs. G. Karakatsanis et al. (2009) investigated voltage over-scaling techniques to optimize RCA performance with minimal impact on accuracy.

3. NAND-Based and Carry-Based Approximate Adders

Harron Waris et al. (2019) proposed NAND-based approximate adders, demonstrating a 29% reduction in critical path delay compared to conventional adders【4】. Additionally, M. Ramasamy et al. (2019) designed carry-based approximate adders, which saved up to 98% power while maintaining reasonable accuracy.

4. Majority Logic-Based Approximate Adders

Recent studies have explored Majority Logic (ML) adders, which optimize area and delay constraints. Zhang et al. (2018) introduced an ML-based approximate full adder, reducing transistor count and power dissipation.

5. Error Metrics in Approximate Adders

Several studies use Mean Error Distance (MED) and Normalized MED (NMED) to evaluate error tolerance in approximate circuits. Researchers conclude that replacing specific bit positions in RCAs with approximate adders provides an optimal trade-off between accuracy and power efficiency.

PROPOSED SYSTEM

In conventional Ripple Carry Adders (RCA), accurate full adders are used to perform binary addition. These adders provide precise outputs but suffer from major drawbacks:

1. High Propagation Delay – Since carry is propagated sequentially through each stage, the delay increases significantly as the number of bits increases.
2. Power Consumption – Accurate adders consume higher power due to the large number of transistors required for precise computation.
3. Area Constraints – The number of logic gates in a full adder increases complexity, making it inefficient for resource-constrained applications.

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4. Inefficiency in Approximate Applications – Many applications like image processing, AI, and DSP can tolerate slight inaccuracies. However, accurate adders consume excessive power even when absolute precision is unnecessary.

To overcome these challenges, researchers have explored approximate computing, which trades accuracy for efficiency, making adders faster and more energy-efficient.

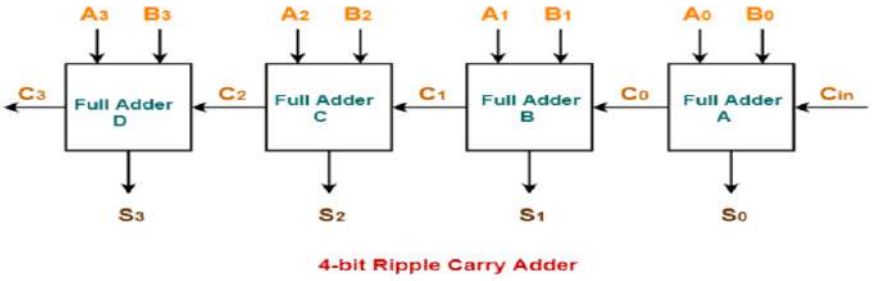

Figure.1 4 bit Ripple carry adder

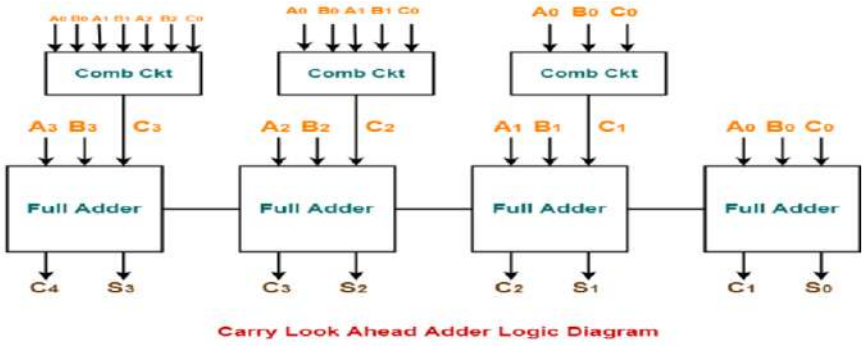

Figure.2 Carry Ahead Adder logic diagram

SIMULATION RESULTS

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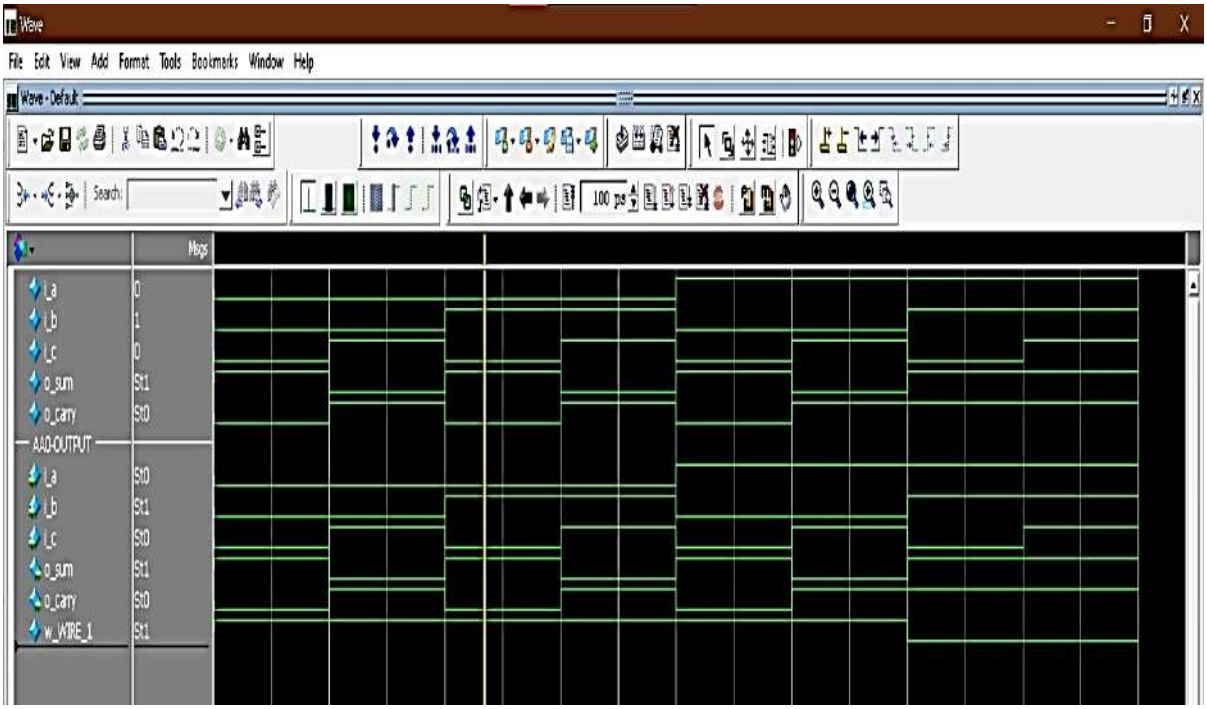

Figure.3 Simulation ResultsAA0

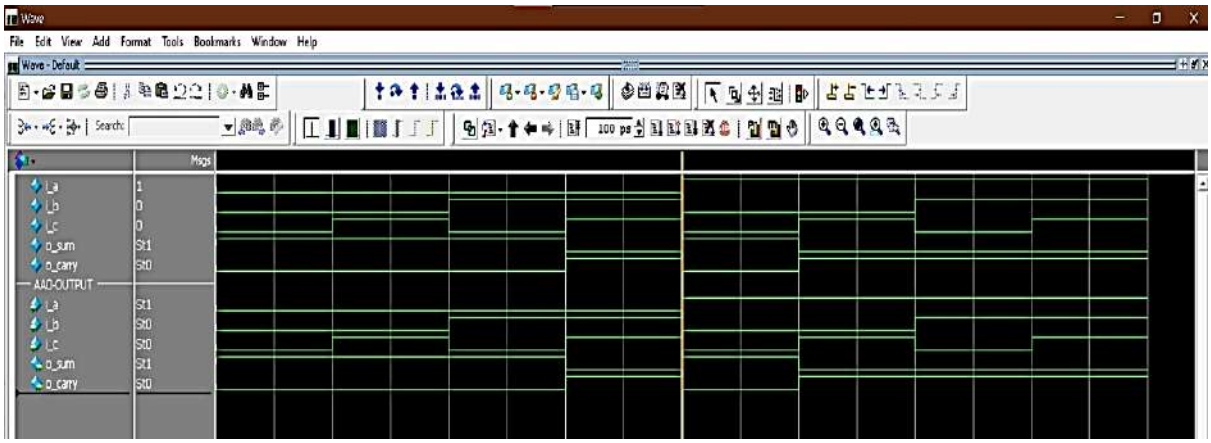

Figure.4 Simulation Results AA5

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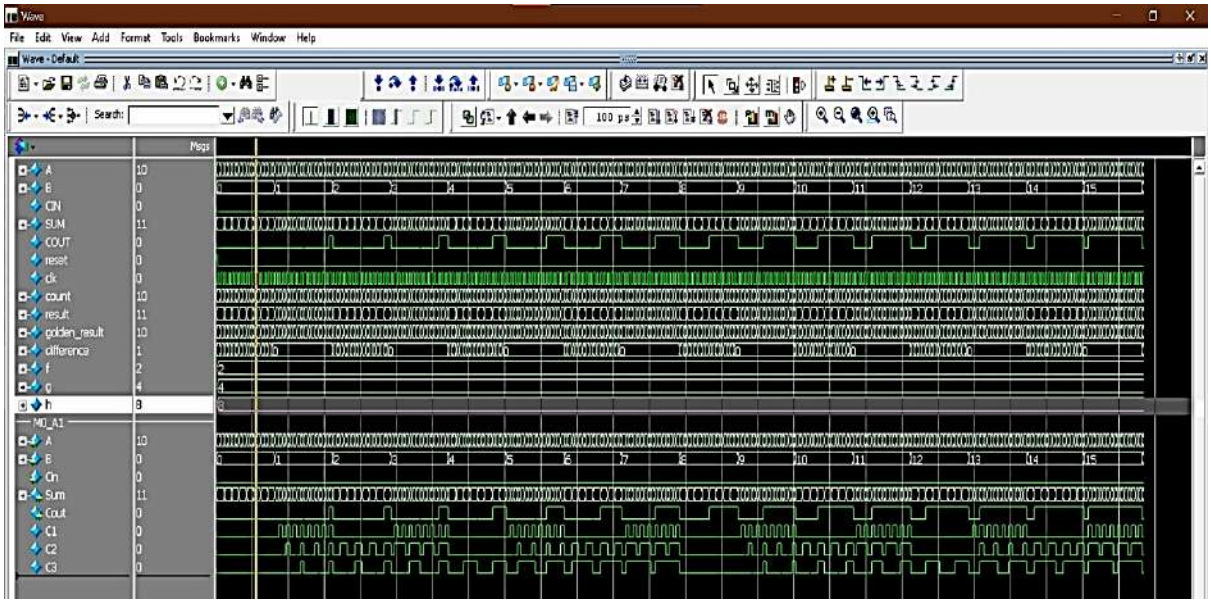

Figure.5 Simulation Results M0-AA1

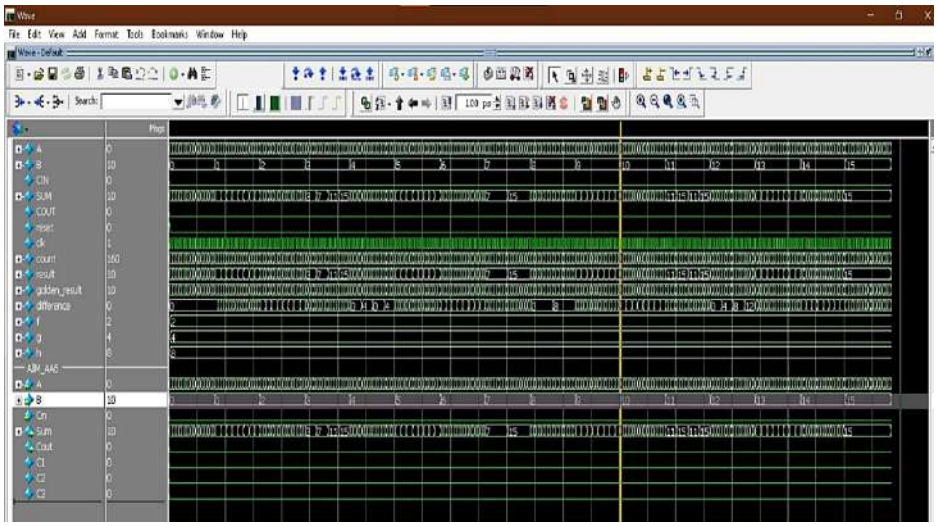

Figure.6 Results ALL_M-AA6

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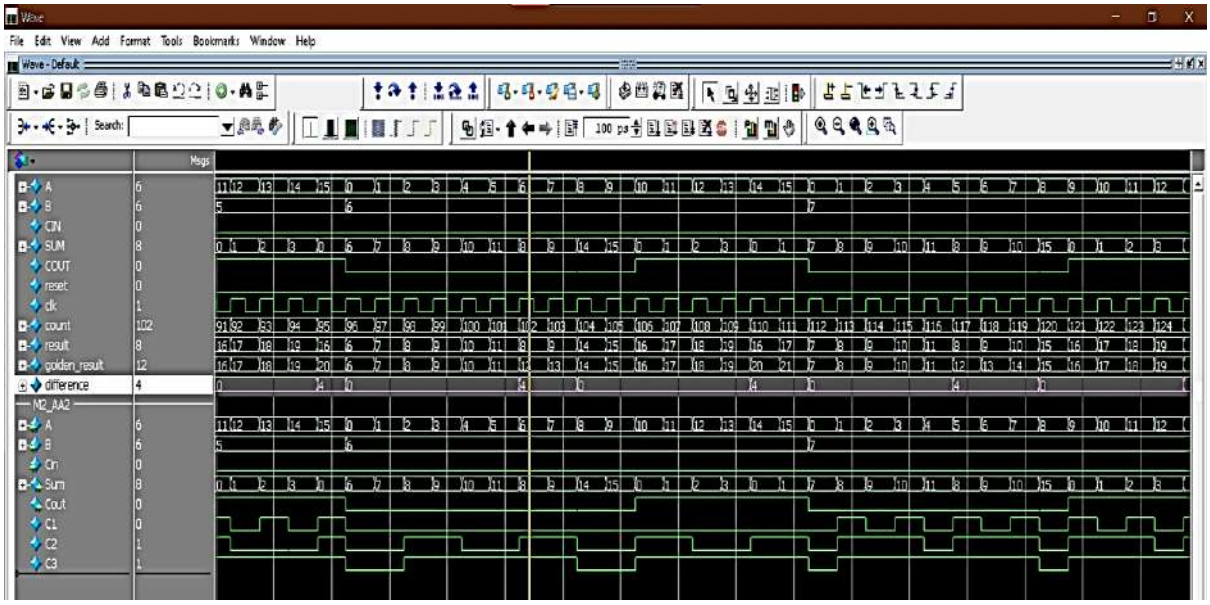

Figure.7Simulation Results M2-AA6

APPROXIMATE ADDER	M0	M2	M3	M1_M2	ALL M
AA0	37.5	37.5	37.5	59.37	81.05
AA1	37.5	37.5	37.5	62.5	87.5
AA2	37.5	37.5	37.5	59.37	82.61
AA3	37.5	37.5	37.5	59.37	82.61
AA4	25	25	25	43.75	68.35
AA5	25	25	25	43.75	68.35
AA6	25	25	25	43.75	68.35

Table.1 Error Percentages

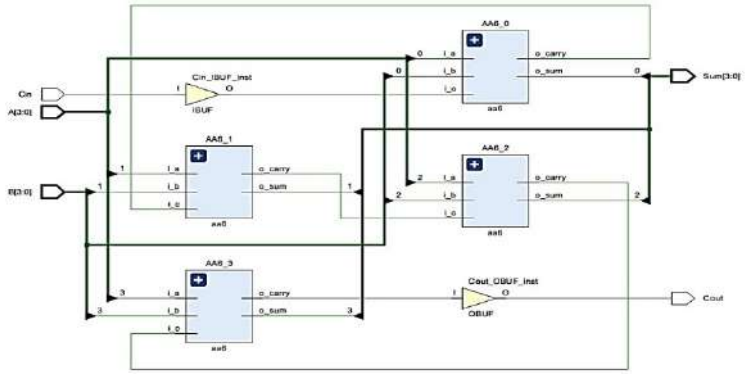

Figure.8 Schematic All_M_AA6

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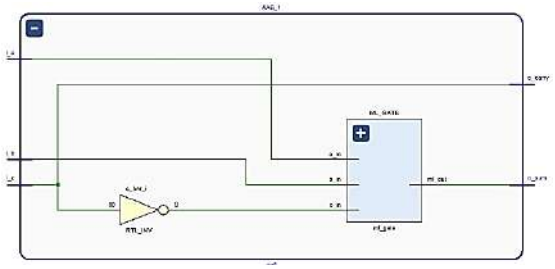

Figure.9 Schematic AA6

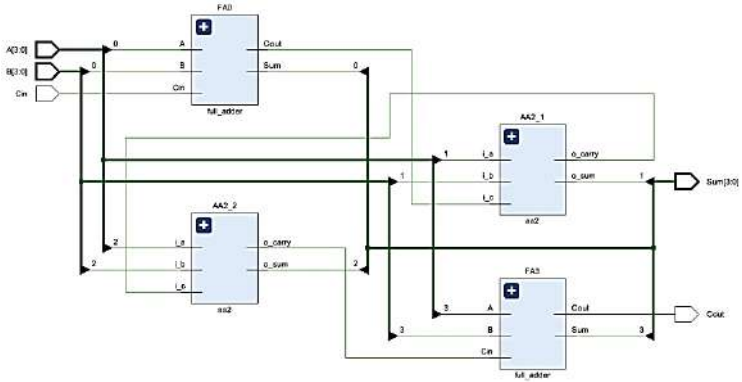

Figure.10 Schematic M1_M2_AA2

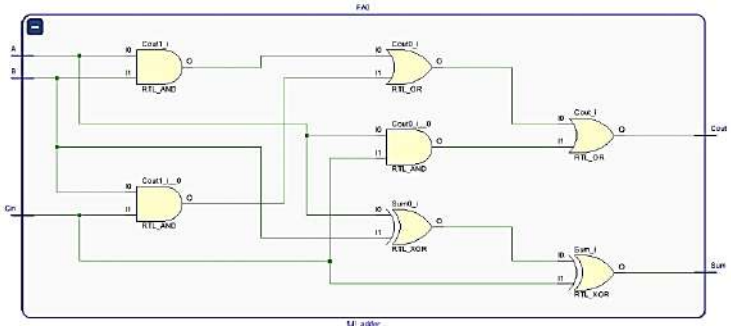

Figure.11 Schematic AA2

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	4	0	303600	<0.01
LUT as Logic	4	0	303600	<0.01
LUT as Memory	0	0	130800	0.00
Slice Registers	0	0	607200	0.00
Register as Flip Flop	0	0	607200	0.00
Register as Latch	0	0	607200	0.00
F7 Muxes	0	0	151800	0.00
F8 Muxes	0	0	75900	0.00

Figure.12 Area Report All_M_AA6

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Site Type	Used	Fixed	Available	Util%
Slice LUTs*	4	0	303600	<0.01
LUT as Logic	4	0	303600	<0.01
LUT as Memory	0	0	130800	0.00
Slice Registers	0	0	607200	0.00
Register as Flip Flop	0	0	607200	0.00
Register as Latch	0	0	607200	0.00
F7 Muxes	0	0	151800	0.00
F8 Muxes	0	0	75900	0.00

Figure.13 Area Report M1_M2_AA2

```
Max Delay Paths
--------------------------------------------------------------------------------------
Slack (MET) :             0.761ns  (required time - arrival time)
  Source:                 A[0]
                            (input port)
  Destination:            Sum[0]
  Path Group:             **default**
  Path Type:              Max at Slow Process Corner
  Requirement:            5.000ns  (MaxDelay Path 5.000ns)
  Data Path Delay:        4.239ns  (logic 3.071ns (72.464%)  route 1.167ns (27.536%))
  Logic Levels:           3  (IBUF=1 LUT3=1 OBUF=1)
  Output Delay:           0.000ns
  Timing Exception:       MaxDelay Path 5.000ns
```

Figure.14 Max path Delay All_M_AA6

```
Max Delay Paths
--------------------------------------------------------------------------------------
Slack (MET) :             0.335ns  (required time - arrival time)
  Source:                 A[0]
                            (input port)
  Destination:            Sum[3]
  Path Group:             **default**
  Path Type:              Max at Slow Process Corner
  Requirement:            5.000ns  (MaxDelay Path 5.000ns)
  Data Path Delay:        4.665ns  (logic 3.139ns (67.304%)  route 1.525ns (32.696%))
  Logic Levels:           4  (IBUF=1 LUT5=2 OBUF=1)
  Output Delay:           0.000ns
  Timing Exception:       MaxDelay Path 5.000ns
```

Figure.15 Max path Delay M1_M2_AA2

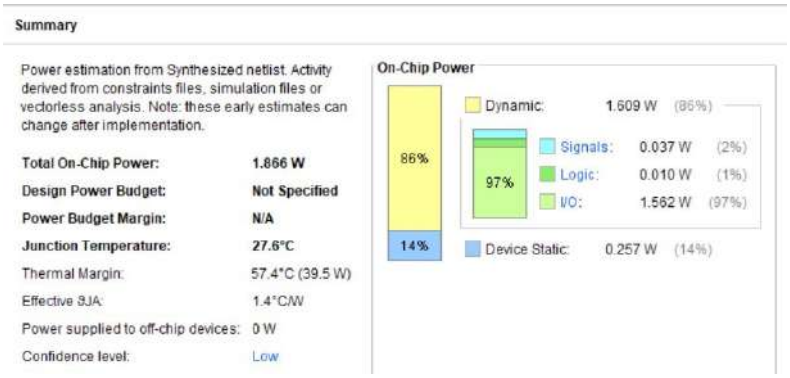

Figure.16 Power Summary ALL_M_AA6

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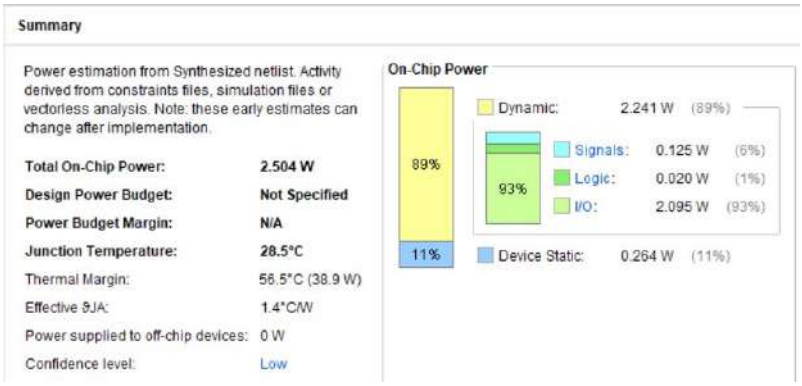

Figure.17 Power Summary M1_M2_AA6

ADVANTAGES

1. Power Efficiency

- Approximate adders reduce power consumption by simplifying logic gate structures.
- Carry-based and NAND-based approximate adders have shown up to 98% power savings compared to traditional adders.

2. Reduced Circuit Complexity

- The replacement of conventional full adders with approximate adders lowers transistor count, reducing the overall circuit area.
- Majority Logic (ML) based adders further optimize the hardware complexity while maintaining performance.

3. Improved Speed & Reduced Propagation Delay

- Ripple Carry Adders (RCAs) suffer from high carry propagation delay.
- Approximate adders help in minimizing critical path delay, making them suitable for high-speed applications.

4. Error-Tolerant Applications

- In domains like image processing, multimedia, and deep learning, minor computational errors do not significantly impact performance.
- The use of Mean Error Distance (MED) and Normalized MED (NMED) ensures that errors remain within acceptable limits.

5. Cost Reduction

- Fewer logic gates and optimized power consumption reduce fabrication costs in large-scale VLSI chip designs.

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APPLICATIONS

1. Image and Video Processing

- Approximate adders are extensively used in image filtering, compression, and enhancement algorithms where slight inaccuracies do not significantly affect visual quality.
- Video encoding standards like JPEG and MPEG allow a certain level of error, making approximate computing an ideal choice for reducing energy consumption.

2. Machine Learning and Deep Learning

- Many machine learning models, especially neural networks, rely on massive matrix multiplications and additions.
- Approximate adders help optimize hardware accelerators like TPUs (Tensor Processing Units) and GPUs, improving efficiency in AI inference and training.

3. Digital Signal Processing (DSP)

- DSP applications such as audio processing, noise reduction, and speech recognition can tolerate minor computational errors.
- Approximate adders reduce power consumption in devices like smartphones, hearing aids, and voice assistants.

4. Internet of Things (IoT) and Edge Computing

- Low-power IoT devices, including smart sensors, wearable electronics, and edge AI devices, require efficient computing with minimal energy usage.
- Approximate computing extends battery life in embedded systems and real-time applications.

5. Cryptography and Security

- Some cryptographic algorithms use low-power approximate adders for efficient encryption and decryption.
- Secure hardware implementations can leverage approximate adders to balance power efficiency and performance.

CONCLUSION

In this project, we have analysed the impact of various approximate adders on Ripple Carry Adder (RCA) design, focusing on power efficiency, delay reduction, and area constraints. The study examined different approximate full adder architectures, including NAND-based, carry-based, and majority logic-based adders, and their integration into 4-bit and 8-bit RCA circuits.

The results indicate that replacing conventional full adders with approximate adders in selective bit positions can significantly reduce design complexity while maintaining an acceptable error percentage. However, when all bit positions are replaced with approximate adders, the error accumulation increases, impacting overall accuracy. Through error metrics such as Mean Error Distance (MED) and Normalized MED (NMED), we evaluated the trade-offs between performance and precision.

ISSN 2319-5991 www.ijerst.com

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The key findings suggest that approximate adders are highly beneficial in applications where absolute accuracy is not a priority, such as image processing, deep learning, and IoT devices. By strategically replacing specific bit positions in RCAs, we achieve optimized power consumption and reduced propagation delay, making them ideal for low-power VLSI systems.

Future research can extend this work by implementing higher-bit adders or integrating approximate adders in other arithmetic units such as multipliers and ALUs. Additionally, exploring adaptive approximate computing techniques could further enhance efficiency while maintaining dynamic accuracy based on application requirements.

Overall, this study reinforces the importance of approximate computing in modern digital design, paving the way for more energy-efficient, high-performance computing architectures.

FUTURE SCOPE

1. Optimization for Higher-Order Adders

- The current study focuses on 4-bit and 8-bit RCAs, but future work can extend the design to higher-bit adders (16-bit, 32-bit, or 64-bit) used in complex digital processing systems.
- Optimizing approximate adders for large-scale arithmetic operations will enhance performance in AI accelerators and signal processing units.

2. Integration into Advanced VLSI Circuits

- Approximate adders can be integrated into ASIC (Application-Specific Integrated Circuits) and FPGA (Field-Programmable Gate Arrays) to improve energy efficiency.
- Their implementation in low-power microprocessors and DSPs can revolutionize embedded systems and edge computing.

REFERENCES

1. V. K. Chippa, S. T. Chakradhar, K. Roy, and A. Raghunathan, "Analysis and Characterization of Inherent Application Resilience for Approximate Computing," in Proceedings of the 50th Annual Design Automation Conference
2. J. Schlachter, B. Reddy, and A. Burg, "Design and Applications of Approximate Circuits by Gate-Level Pruning," in IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, vol. 25, no. 5, 2017. [DOI: 10.1109/TVLSI.2017.2657799]
3. G. Karakatsanis, D. Mohapatra, and K. Roy, "System-Level DSP Synthesis Using Voltage Over-Scaling, Unequal Error Protection, and Adaptive Quality Tuning," in Proceedings of the IEEE Workshop on Signal Processing Systems, 2009. [DOI: 10.1109/SIPS.2009.5336253]
4. H. Waris, C. Wang, and W. Liu, "High-Performance Approximate Half and Full Adder Cells Using NAND Logic Gate," in IEICE Electronics Express, vol. 16, no. 6, 2019. [DOI: 10.1587/elex.16.20190361]

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 21, Issue 1, 2025

5. M. Ramasamy, G. Narmadha, and S. Deivasigamani, "Carry-Based Approximate Full Adder for Low Power Approximate Computing," in 7th International Conference on Smart Computing & Communications
6. T. Zhang, W. Liu, and M. O'Neill, "Design of Majority Logic (ML)-Based Approximate Full Adders," in Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), 2018. [DOI: 10.1109/ISCAS.2018.8350962]
7. Z. Chu, C. Shang, and L. Wang, "Efficient Design of Majority-Logic-Based Approximate Arithmetic Circuits," in IEEE Transactions on VLSI Systems, vol. 30, no. 12, 2022. [DOI: 10.1109/TVLSI.2022.3210252]
8. P. Lagidi, A. Iswarya, G. Rajesh, and A. S. Keerthi Nayani, "Design of 16-Bit and 32-Bit Approximate Full Adder Using Majority Logic," in IEEE Global Conference for Advancement in Technology (GCAT), Bangalore, India, 2021. [DOI: 10.1109/GCAT52182.2021.9587782]
9. N. Maheshwari, Z. Yang, J. Han, and F. Lombardi, "A Design Approach for Compressor-Based Approximate Multipliers," in 28th International Conference on VLSI Design, 2015. [DOI: 10.1109/VLSID.2015.59]