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DESIGN OF 64-BIT SIGNED MAGNITUDE COMPARATOR USING FPGA FOR IOT APPLICATIONS

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ABSTRACT

The increasing demand for high-speed and efficient data processing in IoT applications necessitates the development of optimized hardware comparators. This project presents a Novel High-Speed 64-bit Signed Magnitude Comparator (SMC) designed using Verilog HDL, targeting applications such as sorting techniques, digital communication devices, data converters, and processor address decoding units. The proposed design follows a hierarchical approach, where the Most Significant Bit (MSB) of two 64-bit signed numbers, represented in two's complement form, is compared first, followed by the remaining bits to determine whether the numbers are equal, greater, or lesser. The 8-bit signed comparator serves as the fundamental building block (Leaf Cell) of the design and is hierarchically extended to 16-bit, 32-bit, and finally 64-bit using structural modelling in Verilog HDL. The proposed 64-bit SMC achieves a significantly less delay, demonstrating its efficiency in high-speed computation. The design has been functionally verified, synthesized, and implemented in Xilinx Vivado

INTRODUCTION

The increasing demand for high-speed digital processing in Internet of Things (IoT) applications necessitates efficient arithmetic circuits, particularly for sorting, searching, and data conversion tasks. Among these, comparators play a crucial role in decision-making processes within processors, communication systems, and memory architectures. Traditional unsigned magnitude comparators are widely used, but they are inadequate for signed number operations, which are essential in numerous real-world applications. The Signed Magnitude Comparator (SMC) provides an effective solution for comparing signed binary numbers, making it a key component in high-performance computing and digital signal processing.

This paper presents a 64-bit Signed Magnitude Comparator (SMC) implemented using Field Programmable Gate Arrays (FPGA) to enhance computational efficiency in IoT-based applications. The design leverages Verilog HDL and employs a hierarchical approach, starting from an 8-bit signed comparator and scaling up to 64-bit using structural modeling techniques. The comparison process is optimized by first analyzing the Most Significant Bit (MSB), which represents the sign of the number, followed by a magnitude-based evaluation.

This approach significantly reduces computational delay and improves overall system performance.

The proposed 64-bit SMC is synthesized and implemented on the Xilinx Artix-7 FPGA (XC7A100TCSG324C-3) using Vivado 2012.3. Performance metrics such as delay, power consumption, and area utilization are analyzed to validate the efficiency of the design.

Experimental results indicate that the comparator achieves a delay of 8.239 ns, demonstrating its capability for high-speed applications.

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The development of an efficient signed magnitude comparator has broad implications for sorting algorithms, address decoding, and digital communication systems. By optimizing the comparator's architecture, this work contributes to advancing FPGA-based computing solutions, particularly in resource-constrained IoT environments where speed and power efficiency are critical.

LITERATURE SURVEY

"A Novel Approach for Signed Number Comparison" by Shun-Wen Cheng et al. (2003):

This paper presents a high-speed magnitude comparator architecture optimized for signed numbers. The authors propose a hardware-based algorithm that prioritizes sign- bit comparison, thereby reducing delay in cases where the sign bits differ. The study highlights the importance of low-power arithmetic circuits for real-time applications such as embedded systems and signal processing.

"Efficient Comparator Designs for Residue Number System (RNS)" by Y.WANG ET AL. (1999):

This research focuses on signed number comparison using residue arithmetic. The authors develop a new Chinese Remainder Theorem (CRT) II-based method to perform high-speed comparisons in RNS. The paper discusses trade-offs between hardware complexity and computational efficiency, highlighting the advantages of modular architectures for large-scale arithmetic computations.

"High-Speed FPGA-Based Sorting Using Optimized Comparators" by B. Zarei et al. (2010):

This paper explores the role of magnitude comparators in high-performance sorting. The authors implement parallel comparator architectures using FPGA, demonstrating improved latency and power consumption compared to traditional software-based sorting techniques. The work emphasizes the importance of hardware-efficient comparator designs in applications like big data processing and AI accelerators.

"Fast and Area-Efficient Magnitude Comparator Design" by Reto Zimmermann et al. (1999):

This paper presents an optimized hardware design for magnitude comparators with a focus on reducing area and logic depth. The authors propose parallel prefix logic to minimize delay and evaluate different implementations on FPGA and ASIC platforms. Their findings demonstrate a trade-off between speed and power efficiency, making their approach suitable for high-performance computing applications.

PROPOSED SYSTEM

The proposed system introduces an efficient design for a fixed-width adder tree, addressing the limitations of the existing full-width adder tree architecture. The key innovation lies in optimizing the adder tree structure to achieve improved performance and versatility, particularly in applications with specific fixed-width requirements.

Unlike the existing system, which processes input operands of full width in each adder stage, the proposed system focuses on designing adder stages tailored to handle fixed-width inputs. By customizing the adder stages to match the required operand size, the proposed system reduces unnecessary overhead and improves overall efficiency.

Additionally, the proposed system incorporates techniques to enhance scalability and adaptability. It allows for easy expansion or contraction of the adder tree structure to accommodate varying fixed- width requirements, ensuring optimal performance across a range of applications.

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Furthermore, the efficient design of the fixed-width adder tree in the proposed system helps minimize power consumption and area utilization, making it suitable for low-power and resource-constrained environments.

1-Bit Magnitude Comparator

A comparator used to compare two bits is called a single-bit comparator. It consists of two inputs each for two single-bit numbers and three outputs to generate less than, equal to, and greater than between two binary numbers. The truth table for a 1-bit comparator is given below.

A	B	A<B	A=B	A>B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

Figure.1 1-bit Comparator

From the above truth table logical expressions for each output can be expressed as follows.A>B: AB' A<B: A'B A=B: A'B' + ABBy using these Boolean expressions, we can implement a logic circuit for this comparator as given below.

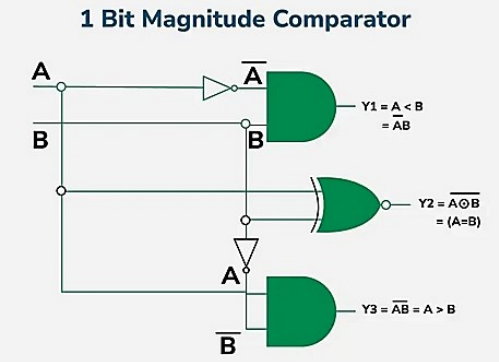

Figure.2 Circuit Diagram 1-bit Comparator

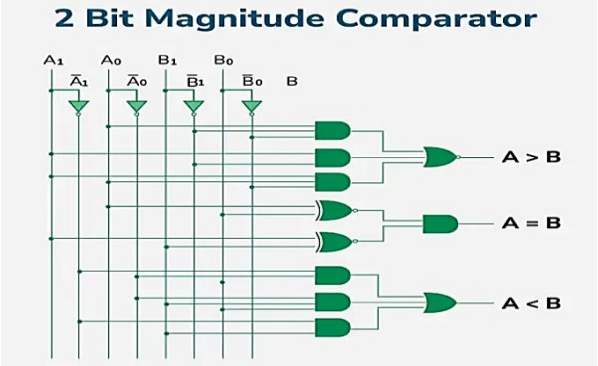

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Figure.3 Circuit Diagram of 2bit Comparator

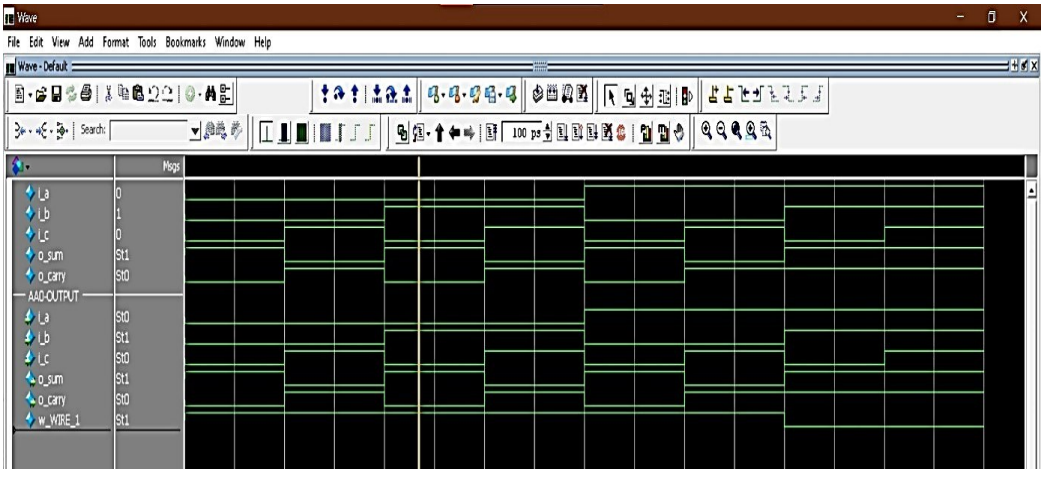
A comparator used to compare two binary numbers each of two bits is called a 2-bit Magnitude comparator. It consists of four inputs and three outputs to generate less than, equal to, and greater than between two binary numbers.

By using these Boolean expressions, we can implement a logic circuit for this comparator as given below.

INPUT				OUTPUT		
A1	A0	B1	B0	A<B	A=B	A>B
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

Figure.4 Truth Table

SIMULATION RESULTS



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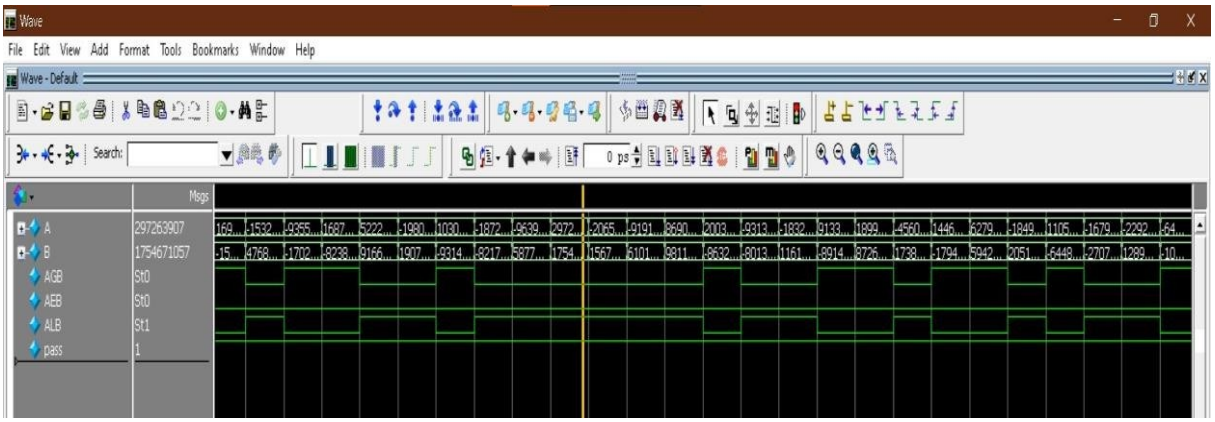

Figure.6 Simulation result of 32-bit SMC

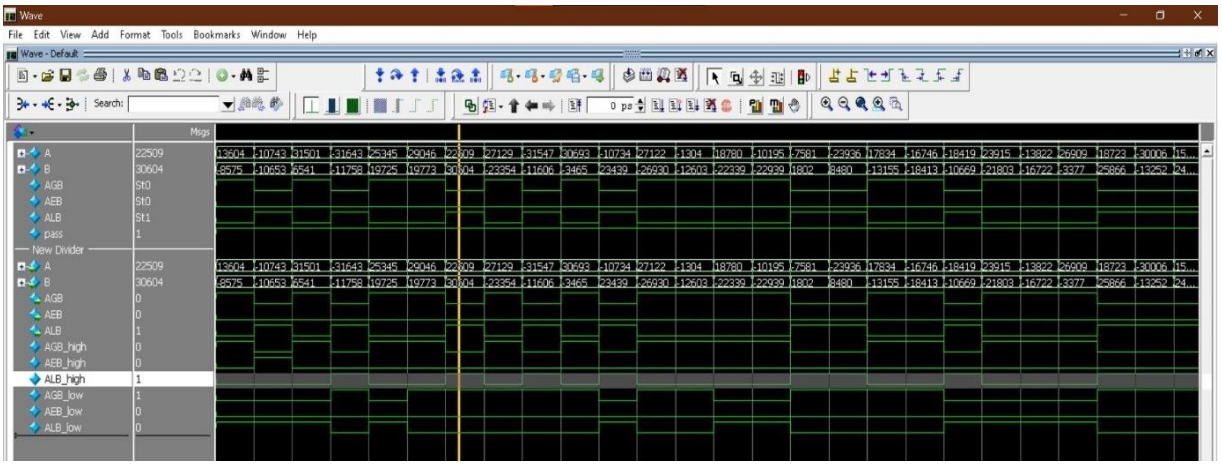

Figure.7 Simulation result of 16-bit SMC

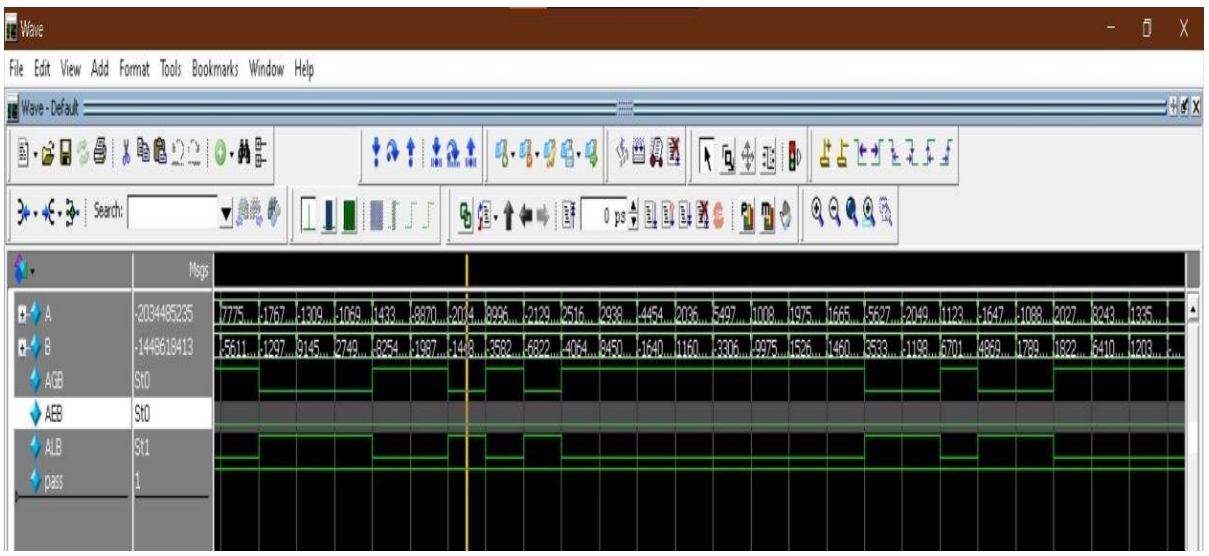

Figure.8 Simulation output

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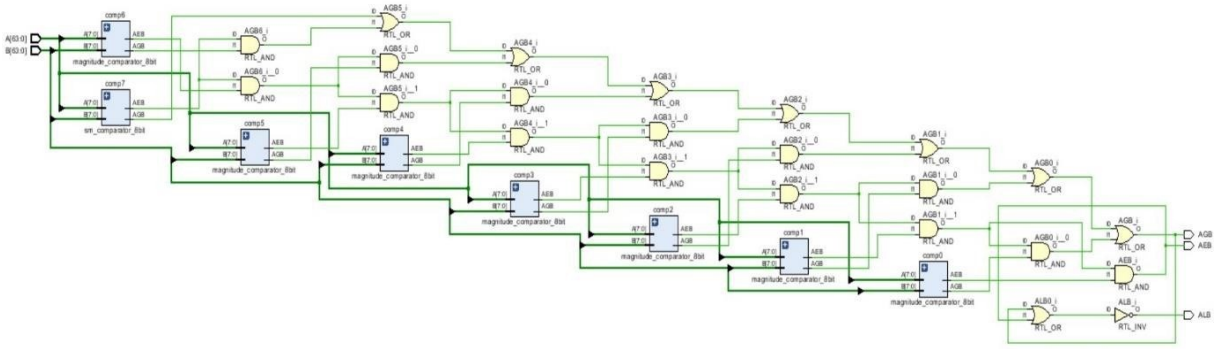

Figure.9 RTL Schematic 64Bit SMC

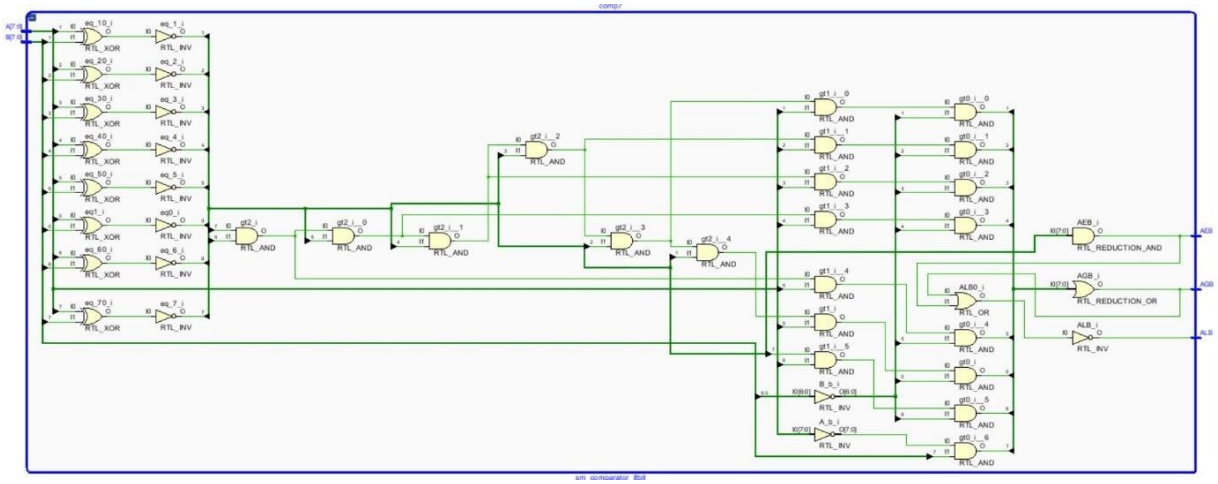

Figure.10 RTL Schematic 64Bit SMC

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	19	0	63400	0.03
LUT as Logic	19	0	63400	0.03
LUT as Memory	0	0	19000	0.00
Slice Registers	0	0	126800	0.00
Register as Flip Flop	0	0	126800	0.00
Register as Latch	0	0	126800	0.00
F7 Muxes	0	0	31700	0.00
F8 Muxes	0	0	15850	0.00

Figure.11 Area Report 16-Bit SMC

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Site Type	Used	Fixed	Available	Util%
Slice LUTs*	11	0	63400	0.02
LUT as Logic	11	0	63400	0.02
LUT as Memory	0	0	19000	0.00
Slice Registers	0	0	126800	0.00
Register as Flip Flop	0	0	126800	0.00
Register as Latch	0	0	126800	0.00
F7 Muxes	0	0	31700	0.00
F8 Muxes	0	0	15850	0.00

Figure.12 Area Report 8-Bit SMC

```
Max Delay Paths
--------------------------------------------------------------------------------
Max Delay Paths
--------------------------------------------------------------------------------
Slack (MET) :             3.628ns  (required time - arrival time)
  Source:                 B[28]
                            (input port)
  Destination:            AGB
  Path Group:             **default**
  Path Type:              Max at Slow Process Corner
  Requirement:            10.000ns  (MaxDelay Path 10.000ns)
  Data Path Delay:        6.372ns  (logic 3.481ns (54.627%)  route 2.891ns (45.373%))
  Logic Levels:           6  (IBUF=1 LUT2=1 LUT6=3 OBUF=1)
  Output Delay:           0.000ns
  Timing Exception:       MaxDelay Path 10.000ns
```

Figure.13 Max Delay 32-bit SMC

```
Max Delay Paths
--------------------------------------------------------------------------------
Max Delay Paths
--------------------------------------------------------------------------------
Slack (MET) :             4.872ns  (required time - arrival time)
  Source:                 B[5]
                            (input port)
  Destination:            AGB
  Path Group:             **default**
  Path Type:              Max at Slow Process Corner
  Requirement:            10.000ns  (MaxDelay Path 10.000ns)
  Data Path Delay:        5.128ns  (logic 3.369ns (65.694%)  route 1.759ns (34.306%))
  Logic Levels:           5  (IBUF=1 LUT2=1 LUT6=2 OBUF=1)
  Output Delay:           0.000ns
  Timing Exception:       MaxDelay Path 10.000ns
```

Figure.14 Max Delay 8-bit SMC

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ADVANTAGES:

High-Speed Operation

The proposed hierarchical cascading approach minimizes delay by prioritizing sign-bit evaluation before magnitude comparison.

Achieves a total delay of 8.239 ns, making it faster than traditional signed comparators.

Optimized for Signed Number Comparison

Unlike conventional unsigned magnitude comparators, this design efficiently compares signed numbers using a signed magnitude representation.

Eliminates the need for additional conversions from two's complement format.

FPGA Implementation for Real-Time Applications

Designed and synthesized for Artix-7 FPGA, ensuring practical applicability in embedded systems.

FPGA-based implementation provides low latency and high throughput for real- time processing.

Reduced Power Consumption

The design enables selective activation of submodules, reducing dynamic power dissipation.

Only the necessary 8-bit comparator blocks are activated based on sign-bit differences, minimizing unnecessary computations.

APPLICATIONS

Sorting Algorithms and Data Processing

Used in high-speed sorting algorithms for arranging large datasets efficiently.

Essential for parallel sorting hardware accelerators in AI and machine learning.

Digital Signal Processing (DSP)

Enhances real-time signal comparison in audio, image, and video processing

IoT Edge Computing

Used in low-power IoT devices for fast numerical comparisons with minimal energy consumption.

Helps in sensor data processing and decision-making in edge devices.

Artificial Intelligence and Machine Learning Accelerators

Optimizes hardware-accelerated AI inference engines by reducing comparison latency.

Useful in decision trees and classification algorithms where numerical comparisons are frequent.

Cryptographic Systems

Helps in public key cryptography and digital signature verification where large number comparisons are required.

Supports secure multiparty computations (MPC)by enabling efficient comparison of encrypted values.

CONCLUSION

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The 64-bit Signed Magnitude Comparator (SMC) has been successfully implemented on an Artix-7 FPGA, achieving high-speed performance. The proposed design enhances comparison efficiency for signed binary numbers by utilizing a gating circuit, making it well-suited for IoT applications. By leveraging sign-bit evaluation, the architecture significantly reduces delay, as only the necessary sub-blocks are activated when sign bits are equal, minimizing unnecessary computations.

This design is particularly effective for Residue Number Systems (RNS) and sorting applications, where high-speed numerical comparison is crucial. The scalability of the proposed model allows it to be extended to 128-bit precision based on application needs. Additionally, further optimizations can be made to reduce power consumption by enabling only the required comparators when sign bits differ, thereby minimizing standby power dissipation.

Beyond FPGA implementation, this design can also be adapted for ASIC development. A 4- bit SMC could be initially designed using universal gates and extended up to 64-bit using a cascading approach. At the CMOS logic level, optimizing parameters such as fan-out and Figure of Merit could further enhance performance and power efficiency for ASIC-based SMCs.

FUTURE SCOPE

Higher Precision Comparators (128-bit and Beyond)

The current design can be extended to 128-bit or higher precision for advanced computing applications requiring large number comparisons.

This would be beneficial for scientific computing, high-performance computing (HPC), and cryptographic algorithms.

Power Optimization for Low-Power Applications

Further power reduction strategies, such as clock gating, dynamic voltage scaling, and approximate computing, can be integrated to minimize energy consumption.

This will make the design more suitable for battery-operated IoT devices and edge computing applications.

REFERENCES

1. B. Jeevan and K. Sivani, "Design of 64-bit Signed Magnitude Comparator using FPGA for IoT applications," Proceedings of the International Conference on Advances in Computing, Communication and Applied Informatics (ACCAI), IEEE, 2022. DOI: 10.1109/ACCAI53970.2022.9752617
2. D. Knuth, "Sorting and Searching," The Art of Computer Programming, Vol. 3, Addison-Wesley, 1973.
3. K. Hwang, "Computer Arithmetic: Principles, Architecture, and Design," John Wiley & Sons, 1979.
4. S.-W. Cheng, "A High-Speed Magnitude Comparator with Small Transistor Count," Proceedings of the IEEE International Conference on Electronics, Circuits and Systems (ICECS), pp. 1168-1171, 2003. DOI: 10.1109/ICECS.2003.1301877

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

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5. Y. Wang, X. Song, and M. Abdulhamid, "A New Algorithm for RNS Magnitude Comparison Based on the Chinese Remainder Theorem," Great Lakes Symposium on VLSI (GLSVLSI), pp. 362-365, March 1999. DOI: 10.1109/GLSV.1999.766319

6. B. Zarei, M. Askar Zadeh, N. Derakhshanfard, and M. Hosseinzadeh, "A High-Speed Residue Number Comparator for the 3-Moduli Set," IEEE International Symposium on Signals, Systems and Electronics, pp. 1-4, 2010. DOI: 10.1109/ISSSE.2010.5607154

7. R. Zimmermann, "Computer Arithmetic: Principles, Architectures, and VLSI Design," ETH Zurich, 1999. Available online

8. M. Xu, Z. Bian, and R. Yao, "Fast Sign Detection Algorithm for the RNS Moduli Set," IEEE Transactions on VLSI Systems, Vol. 22, No. 3, pp. 1-5, 2014. DOI: 10.1109/TVLSI.2014.2312162

9. N. H. E. Weste and K. Eshraghian, "Principles of CMOS VLSI Design," Addison- Wesley, 1993.