International Journal of Engineering Research and Science & Technology

www.ijerst.org

ISSN : 2319-5991

Vol. 22 No. 4 (2026)



ijerst.editor@gmail.com

editor@ijerst.com

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com
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Peer Reviewed, Referred & Indexed Journal

Research Paper

Design and Hardware Implementation of a Low-Power 16-Bit Computational Unit Integrating a Pipelined Vedic Multiplier and Kogge-Stone Adder

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Abstract:

Approximate computing (AC) introduces advantages by relaxing the demand for full accuracy, consequently lowering power consumption and area requirements. The Majority Logic (ML) gate serves as a fundamental logic block in numerous emerging nanotechnologies. This Project proposes ML-based arithmetic circuits, specifically multibit adders and multipliers. These adders are meticulously crafted to prevent the propagation of inaccurate carry-out signals to higher-order computing components, thereby enhancing overall accuracy. For the proposed multiplier, a distinctive Partial Product Reduction (PPR) circuitry is implemented, based on the parallel approximate 6:3 compressor. Extensive analyses of logic implementation costs, error metrics, and layouts are conducted using Majority Logic to assess the efficiency of the adder designs. Experimental results showcase a substantial improvement compared to previous ML-based designs.

1.Introduction:

In recent years, the demand for energy-efficient and high-performance arithmetic circuits has escalated with the proliferation of embedded systems, Internet of Things (IoT) devices, and mobile applications. Traditional arithmetic circuits, while accurate, often suffer from high power consumption and area overhead, posing significant challenges in resource-constrained environments. To address these challenges, approximate computing has emerged as a promising paradigm, offering a trade-off between accuracy and efficiency.

This project focuses on the design and optimization of Majority-Logic-Based Approximate Arithmetic Circuits (MLAACs), which leverage the majority logic gate as the fundamental building block. Majority logic gates exploit the inherent redundancy in arithmetic operations and enable the implementation of approximate arithmetic circuits with reduced hardware complexity and improved energy efficiency.

The primary objective of this project is to develop efficient design methodologies for MLAACs that can deliver competitive performance while significantly reducing power consumption and area overhead compared to their conventional counterparts. By exploiting the inherent error resilience of majority logic-based circuits, we aim to achieve substantial improvements in energy efficiency without compromising the overall accuracy of arithmetic operations.

The project will involve exploring various optimization techniques, including gate-level optimization, circuit-level approximation, and algorithmic optimization, to enhance the efficiency and reliability of MLAACs. Moreover, the project will investigate the trade-offs between accuracy, power consumption, and area overhead to identify the optimal design configurations for different application scenarios.

The proposed research is expected to contribute to the advancement of approximate computing techniques and pave the way for the widespread adoption of energy-efficient arithmetic circuits in diverse computing platforms. The outcomes of this project have the potential to revolutionize the design of arithmetic units in embedded systems,

IoT devices, and low-power computing applications, leading to significant improvements in energy efficiency and overall system performance.

2.Existing System:

Several existing approximate arithmetic circuits, such as MLAFA2121, MLAFA2133, and LSA-MSA, have been proposed in the literature to address the trade-off between accuracy and energy efficiency. These circuits employ various approximation techniques to reduce power consumption and area overhead while maintaining acceptable levels of accuracy. However, they also exhibit certain disadvantages that limit their effectiveness in practical applications.

MLAFA2121 and MLAFA2133 are variants of the Majority Logic-Based Approximate Adders (MLAFA) designed to perform addition with reduced hardware complexity. While these circuits offer significant energy savings compared to exact adders, they introduce noticeable errors in the output due to the approximation techniques employed. Additionally, MLAFA2121 and MLAFA2133 struggle to maintain accuracy when dealing with certain input combinations or data types, limiting their reliability in critical applications.

LSA-MSA (Least Significant Approximate - Most Significant Approximate) is another approximate arithmetic circuit designed to perform addition with reduced precision in the least significant bits. While LSA-MSA effectively reduces power consumption and area overhead, it introduces errors that accumulate over multiple operations, leading to inaccuracies in the final result. Furthermore, the design of LSA-MSA may not be easily scalable to handle larger data sizes or more complex arithmetic operations.

3.PROPOSED APPROXIMATE ADDER AND MULTIPLIER

Constructing multibit approximate adders by cascading smaller bit-width adders often leads to issues with erroneous carry propagation. In contrast to this cascading approach, direct utilization of multibit adders may offer a more effective solution. Utilizing direct methods for synthesis, albeit complex, may prove beneficial, particularly for small-scale circuits, such as through truth table modification. A critical aspect in preventing the propagation of erroneous carries is to minimize the number of intermediate carries.

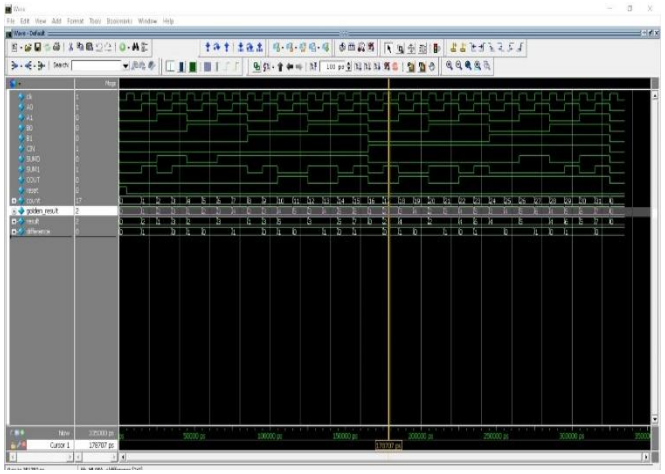
Our primary focus lies in the direct design of 2- and 4-bit approximate adders, with the intention of mitigating the aforementioned issues. For larger bit-widths, such as 8- and 16-bit adders, a cascading approach is proposed by combining the designed 2- or 4-bit adders. Comprehensive evaluations and analyses are conducted for all designs, assessing their performance and identifying any associated errors.

The multiplication process involves three key steps: 1) generating partial products; 2) performing Partial Product Reduction (PPR); and 3) generating final products using Ripple Carry Adders (RCA). PPR significantly impacts latency, power consumption, and design complexity. Integrating appropriate arithmetic blocks, such as compressors, into this stage can notably enhance the efficiency and performance of the multiplier.

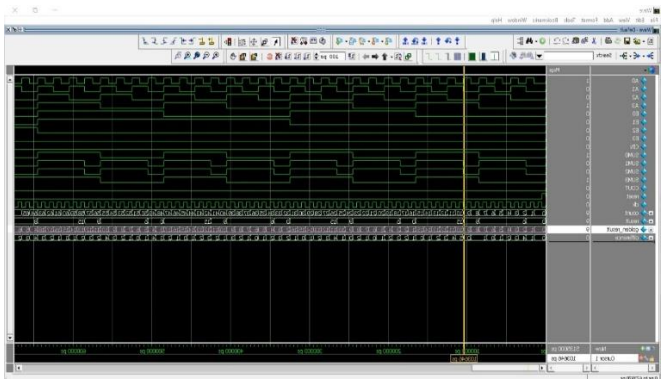
In recent years, there has been a focus on designing imprecise compressors to handle partial products of the same weight. However, only a few compressors are capable of compressing partial products of varying weights simultaneously. For instance, a parallel 10:4 compressor was proposed in [38]. Inspired by this, we introduce an ML-based approximate parallel 6:3 compressor (MLAPC) in this study.

4.SIMULATION RESULTS:

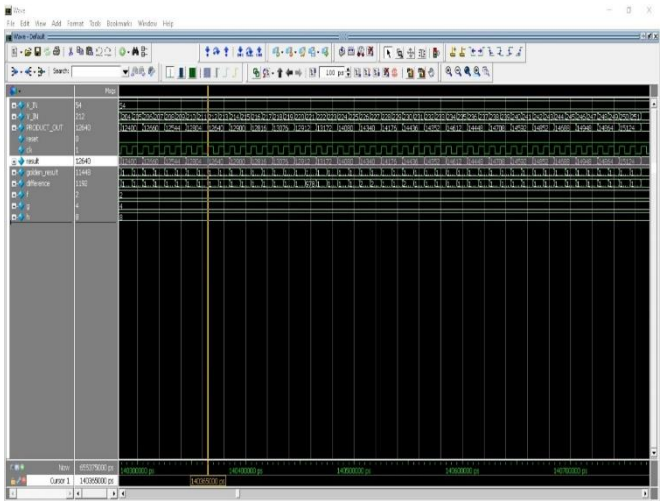
1. MLAFA-a



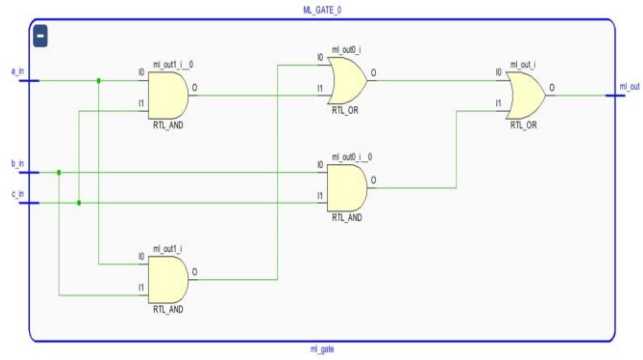
2. MLAFA-1



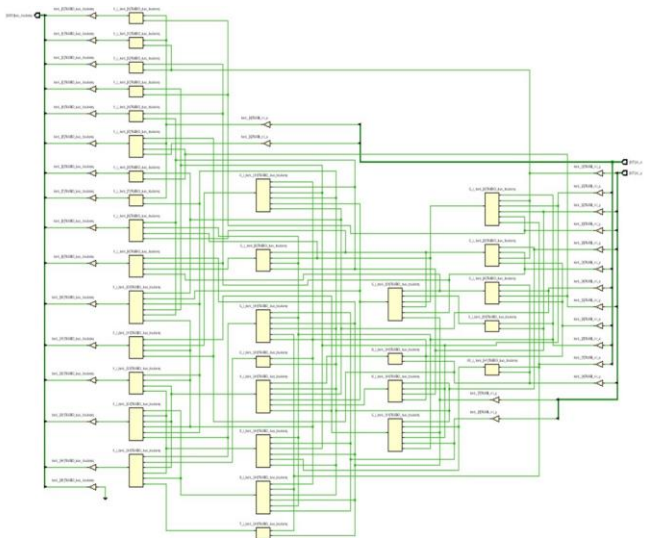
3. 8_8 multiplier



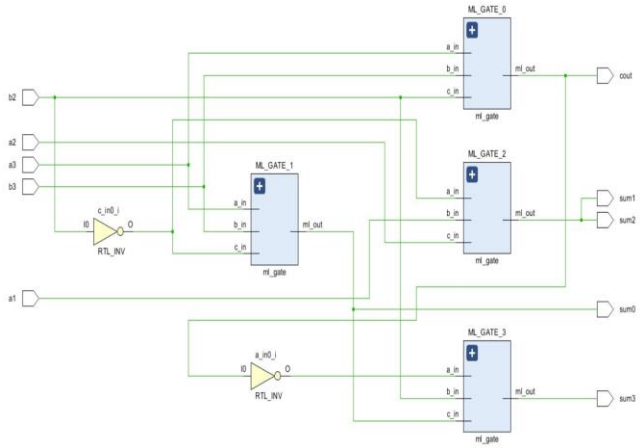
4. ML Gate



5.TECHNOLOGY SCHEMATIC:



6. Schematic Control Unit MLAFA-1



7.Area Report

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	22	0	303600	<0.01
LUT as Logic	22	0	303600	<0.01
LUT as Memory	0	0	130800	0.00
Slice Registers	0	0	607200	0.00
Register as Flip Flop	0	0	607200	0.00
Register as Latch	0	0	607200	0.00
F7 Muxes	0	0	151800	0.00
F8 Muxes	0	0	75900	0.00

Ref Name	Used	Functional Category
OBUF	16	IO
IBUF	16	IO
LUT2	12	LUT
LUT6	11	LUT
LUT4	9	LUT

5.Conclusion and Future Scope

In conclusion, this article has presented innovative designs, thorough analysis, and comprehensive evaluations of approximate adders and multipliers based on Majority Logic (ML). Addressing the limitations of existing approximate adders, the article introduces several 2- and 4-bit adder designs aimed at overcoming these challenges. Additionally, novel contributions include an approximate 6:3 compressor and a unique Parallel Prefix Reduction (PPR) circuit for the parallel compressor in multipliers. These innovations significantly reduce area and delay while maintaining the quality of the multiplier.

Compared to existing approximate designs, the proposed approaches exhibit substantial improvements in logic implementation cost and accuracy. Directly designing multibit approximate adders' results in reduced hardware overhead with lower accuracy loss. The proposed designs show significant reductions in metrics such as Mean Absolute Error (MAE) and Normalized Mean Error Distance (NMED) compared to previous approaches. Furthermore, the proposed approximate adders, leveraging truncated carry chain implementation, outperform other adders implemented by QCA technology.

The proposed PPR circuit showcases superior performance in Majority Logic Approximate Parallel Compression (MLAPC), offering decreased MAE and NMED compared to alternative compressors. It also boasts better hardware overhead metrics. Comparative analysis with exact multipliers reveals significant savings in majority gate usage, inverter utilization, and critical path delay.

The project opens up several avenues for future research and development. Some potential areas for further exploration and enhancement include:

1. Advanced Approximation Techniques: Investigate novel approximation techniques to further optimize the trade-off between accuracy and efficiency in majority-logic-based circuits. This may involve exploring different approximation levels, threshold tuning methods, and adaptive approximation strategies to achieve even greater energy efficiency without compromising performance.
2. Dynamic Approximation Control: Develop dynamic approximation control mechanisms that adaptively adjust the approximation levels of adders and multipliers based on application requirements and workload characteristics. This dynamic control can optimize circuit performance in real-time, maximizing energy efficiency while maintaining acceptable accuracy levels.
3. Error-Tolerant Computing: Explore the integration of majority-logic-based approximate circuits into error-tolerant computing systems. Investigate the potential synergies between approximate computing and error-resilient techniques to design robust and reliable computing systems capable of handling transient errors and environmental variations.
4. Application-Specific Optimization: Explore application-specific optimizations tailored to specific domains such as image processing, machine learning, and signal processing. Investigate how majority-logic-based approximate circuits can be customized and optimized to meet the unique requirements of these applications, enabling even greater energy efficiency and performance gains.
5. Integration with Emerging Technologies: Investigate the integration of majority-logic-based approximate circuits with emerging technologies such as neuromorphic computing, quantum computing, and beyond-CMOS devices. Explore how these circuits can complement and enhance the capabilities of next-generation computing platforms, opening up new opportunities for energy-efficient and high-performance computing.

Overall, the future scope of the project encompasses a wide range of research directions aimed at advancing the state-of-the-art in efficient approximate adders and multipliers circuits. By exploring these avenues, researchers can continue to push the boundaries of energy efficiency and

performance in computing systems, unlocking new opportunities for innovation and impact in various application domains.

6. References

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