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Research Paper

LOW POWER AREA-EFFICIENT 16-BIT ALU WITH LOW-POWER FULL ADDER USING ACCELERATOR

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ABSTRACT

The Arithmetic and Logic Unit (ALU) is a fundamental component of digital processors, embedded systems, controllers, and digital signal processing applications. As computational requirements increase, designing an ALU with reduced power consumption, efficient hardware utilization, and improved processing throughput becomes an important challenge in Very Large-Scale Integration (VLSI) design. Conventional ALU architectures may experience carry propagation delay during arithmetic operations and limited throughput when multiple independent operations are executed sequentially. To address these challenges, this project proposes a low-power-oriented, area-efficient 16-bit ALU using an XNOR-based full-adder formulation and a two-lane hardware accelerator.

The proposed system is developed using a hierarchical architecture consisting of a one-bit full adder, a 16-bit ripple-carry adder, a multifunctional ALU, and two parallel ALU processing lanes. The XNOR-oriented full-adder formulation provides an alternative Boolean representation of conventional sum and carry operations, while the ALU supports arithmetic operations such as addition, subtraction, increment, and decrement, along with logical operations, bit shifting, and comparison functions. The two-lane accelerator enables independent operations to be evaluated concurrently, and a multiplexer selects the required output. The design is described using synthesizable Verilog HDL and is intended for functional verification through Xilinx ISE and ISim tools. Three verification scenarios are considered to test arithmetic operations, logical and shift operations, comparison functions, and parallel accelerator behavior.

The proposed architecture provides a modular and scalable foundation for FPGA-based digital system design, with potential applications in embedded processors, IoT devices, digital signal processing, and hardware acceleration. Its performance can be evaluated using hardware resource utilization, propagation delay, and power estimation. Although parallel processing can improve throughput, duplicating ALU hardware may increase area and active power consumption. Similarly, the XNOR-oriented formulation alone does not guarantee lower power consumption in an FPGA implementation because synthesis tools may map equivalent Boolean expressions into the same

hardware resources. Therefore, comparative synthesis and power analysis under consistent implementation conditions are necessary to establish the actual benefits of the proposed design.

Keywords:
VLSI, Arithmetic and Logic Unit, Low-Power Full Adder, XNOR Logic, Verilog HDL, FPGA, Ripple-Carry Adder, Parallel Accelerator, Area Efficiency, Power Optimization.

I. INTRODUCTION

Very Large-Scale Integration (VLSI) technology plays an important role in the development of modern electronic systems by integrating a large number of transistors and logic circuits onto a single semiconductor chip. The continuous growth of computing applications has increased the demand for digital circuits that provide high performance, low power consumption, and efficient hardware utilization. Arithmetic and Logic Units (ALUs) are essential components of processors, microcontrollers, embedded systems, and digital signal processing devices because they perform arithmetic, logical, and comparison operations. Therefore, designing an ALU with improved processing capability and power-aware architecture is an important area of research in digital VLSI design.

A conventional ALU generally consists of an arithmetic unit, logic circuits, and a selection network that determines the required output based on the operation control signals. The performance of the arithmetic unit depends significantly on the design of the full adder, which is responsible for calculating the sum and carry outputs. In a ripple-carry adder, the carry signal propagates from one bit position to the next, potentially increasing the overall computation delay. In addition, when multiple independent operations must be performed, a single ALU may need separate evaluation cycles, limiting the processing throughput. These challenges motivate the development of alternative arithmetic structures and parallel processing architectures that can improve computational efficiency while considering hardware area and power consumption.

This project proposes a Low Power Area-Efficient 16-Bit ALU with Low-Power Full Adder Using Accelerator. The design incorporates an XNOR-oriented full-adder formulation to represent the sum and carry functions and uses sixteen full-adder stages to construct a 16-bit ripple-carry arithmetic path. The ALU supports arithmetic operations such as addition, subtraction, increment, and decrement, along with logical operations including AND, OR, XOR, and XNOR, bit shifting, and comparison functions. Furthermore, a two-lane hardware accelerator is introduced using two independent ALU units that can evaluate separate operations concurrently. A multiplexer selects the required result from the available processing lanes. The complete architecture is described using synthesizable Verilog HDL and is intended to be verified using Xilinx ISE and ISim simulation tools.The proposed system provides a modular architecture for studying the relationship between arithmetic circuit design, hardware parallelism, and implementation efficiency. Functional verification is performed through separate test scenarios covering arithmetic operations, logical and shift operations, comparisons, and parallel accelerator behavior. Hardware performance can be assessed using synthesis reports, resource utilization, propagation delay, and power estimation. Although the parallel accelerator can improve throughput for independent operations, it may increase hardware area and active power because of duplicated ALU resources. Similarly, the actual low-power advantage of the XNOR-oriented full adder must be established through implementation-level evaluation rather than

assumed from its Boolean representation alone. The project therefore provides a foundation for exploring power-aware and scalable ALU architectures for FPGA-based digital systems and future VLSI implementations.

II. LITERATURE REVIEW

Nookala Venu et al. [1] presented a low-power, area-efficient ALU using XNOR logic and a full-adder circuit. Their work focused on reducing power consumption and circuit area, providing the conceptual foundation for the proposed 16-bit ALU.Suresh Kumar N. and Paramasivam K. [2] investigated low-power full-adder design using 65 nm CMOS technology. Their study evaluated power consumption, propagation delay, and area, highlighting the importance of optimizing arithmetic circuits.Ramesh Jangir and Ramakant Vyas [3] proposed an area-efficient full adder using a three-transistor XNOR cell. Their research explored reducing transistor count and improving circuit efficiency, providing useful background for XNOR-oriented arithmetic design.

D. Anitha et al. [4] studied low-power ALU design under process, voltage, and temperature variations. Their work emphasized evaluating power consumption and delay while maintaining reliable circuit operation under different conditions.M. Kathirvelu and Hima Bindu [5] investigated a hybrid full-adder design combining CMOS and transmission-gate logic. Their research compared power consumption, propagation delay, and circuit area to identify efficient arithmetic circuit implementations.Arindam Baul and Akansha Awasthi [6] examined area-efficient, low-power ALU design. Their study highlighted the importance of optimizing arithmetic and logical operations to improve the efficiency of digital processing systems.The reviewed studies demonstrate the importance of full-adder optimization in low-power VLSI design. Based on these concepts, the proposed project integrates an XNOR-oriented full adder into a 16-bit ALU and introduces a two-lane accelerator for parallel processing. The design uses Verilog HDL and is intended for verification through Xilinx ISE and ISim, with area, delay, and power evaluated separately.

III. EXISTING SYSTEM

The existing system uses a conventional Arithmetic and Logic Unit (ALU) consisting of an arithmetic unit, logical circuits, and a multiplexer for selecting the required output. Arithmetic operations are generally performed using a standard adder, while logical operations are implemented using basic logic gates. In conventional architectures, a single ALU processes one selected operation at a time. The performance of the arithmetic unit depends on the adder structure and the propagation of carry signals between bit positions.

The main limitations of the existing system are increased carry propagation delay in ripple-carry arithmetic circuits, potential power consumption due to switching activity, and limited throughput when multiple independent operations must be performed sequentially. Conventional architectures may also require careful optimization to balance hardware area, processing speed, and power consumption. These limitations motivate the development of a 16-bit ALU incorporating an XNOR-oriented full-adder formulation and a parallel hardware accelerator

IV. PROPOSED SYSTEM

The proposed system presents a low-power-oriented, area-efficient 16-bit Arithmetic and Logic Unit (ALU) integrated with an XNOR-oriented full-adder formulation and a two-lane hardware accelerator. The architecture is developed hierarchically using a one-bit full adder, a 16-bit ripple-carry adder, a

multifunctional ALU, and two parallel ALU units. The XNOR-oriented logic provides an alternative representation of the conventional full-adder functions, while the ALU supports arithmetic operations such as addition, subtraction, increment, and decrement, along with logical operations, shifting, and comparison. The design is implemented using synthesizable Verilog HDL and is intended for functional verification using Xilinx ISE and ISim.

The two-lane accelerator allows two independent ALU operations to be evaluated concurrently using separate operands and operation-selection signals. A multiplexer selects the required result, while the individual lane outputs remain available. This parallel architecture can improve processing throughput when multiple independent operations are required. The proposed design can be evaluated using hardware resource utilization, propagation delay, and power estimation to understand the trade-offs between performance, area, and energy efficiency. However, actual power reduction must be verified through implementation results because parallel ALU units may increase hardware area and active power.

V. METHODOLOGY

The methodology of the proposed system consists of designing a low-power-oriented 16-bit Arithmetic and Logic Unit (ALU) using an XNOR-oriented full-adder formulation and integrating a two-lane hardware accelerator. The design is developed using Verilog HDL and follows a modular approach, allowing each component to be designed and verified independently.

Step 1: Full-Adder Design

The first stage involves designing a one-bit full adder with two input bits \(A\), \(B\), and a carry input \(C_{in}\). The sum and carry outputs are expressed as:

\[Sum=A\oplus B\oplus C_{in} \]

\[C_{out}=AB+C_{in}(A\oplus B) \]

The XNOR-oriented formulation uses the intermediate signal:

\[X=\overline{A\oplus B} \]

The sum can then be represented as:

\[Sum=\overline{X\oplus C_{in}} \]

This formulation is logically equivalent to the conventional full-adder sum function.

Step 2: 16-Bit Ripple-Carry Adder Design

Sixteen one-bit full-adder stages are connected to construct the 16-bit arithmetic unit. Each stage receives a carry input from the preceding stage and generates a carry output for the next stage. This structure supports multi-bit addition, although the carry propagation path can influence the overall delay.

Step 3: ALU Design

The 16-bit ALU is developed by integrating the arithmetic unit, logical circuits, shifting operations, comparison functions, and output-selection logic. Based on the operation-selection signal, the ALU performs addition, subtraction, increment, decrement, AND, OR, XOR, XNOR, pass-A, NOT-A, left shift, right shift, equality, greater-than, and less-than operations. Status flags such as zero, negative, carry, and overflow are generated where applicable.

Step 4: Two-Lane Hardware Accelerator

Two independent 16-bit ALU units are connected to form the accelerator. Each lane receives its own operands and operation-selection signal, enabling both lanes to evaluate different operations concurrently. A two-to-one multiplexer controlled by the lane-selection signal selects the required output, while the individual lane results remain available.

Step 5: Verilog Implementation and Simulation

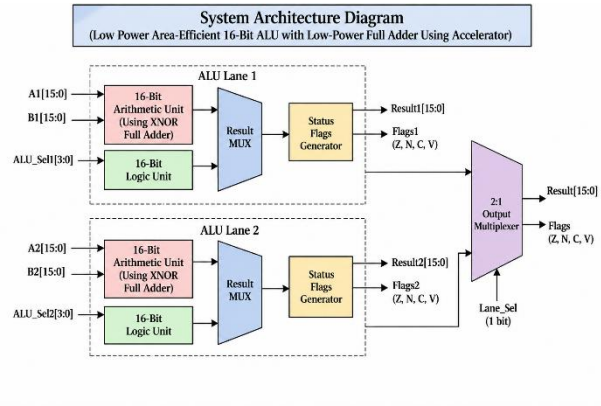
The complete architecture is described using synthesizable Verilog HDL. The modules are integrated hierarchically and prepared for functional verification using Xilinx ISE 13.7 and ISim. Three verification scenarios are considered: arithmetic operations, logical/shift/comparison operations, and parallel accelerator operations. The simulated outputs are compared with the expected results to verify functional correctness.

Step 6: Performance Evaluation

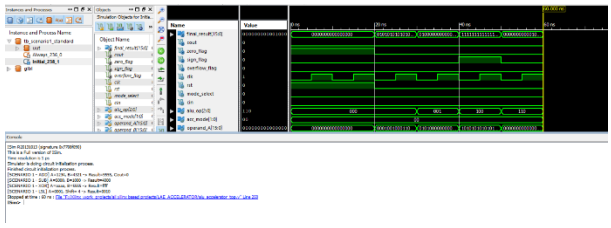
The final stage evaluates the architecture using synthesis and implementation reports. The important parameters include hardware resource utilization, propagation delay, and estimated power consumption. A fair comparison between the conventional ALU and the proposed design requires the same target device and consistent implementation settings. The two-lane accelerator may improve throughput but can increase hardware area and active power. Therefore, the actual low-power and area-efficiency benefits must be established through measured or estimated implementation results rather than assumed from the XNOR logic formulation alone.

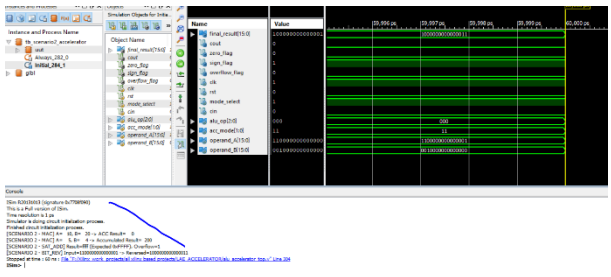
VI. SYSTEM MODEL

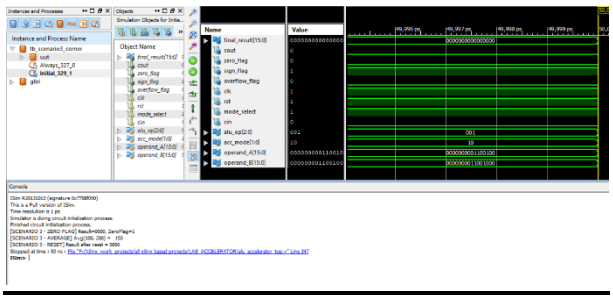
System Architecture



VII. RESULTS AND DISCUSSIONS







VIII. CONCLUSION

The project presents a low-power-oriented, area-efficient 16-bit Arithmetic and Logic Unit (ALU) using an XNOR-oriented full-adder formulation and a two-lane hardware accelerator. The proposed architecture integrates a one-bit full adder, a 16-bit ripple-carry adder, arithmetic and logical operation units, and parallel ALU processing lanes. It supports various operations, including addition, subtraction, increment, decrement, logical operations, shifting, and comparison. The design is developed using synthesizable Verilog HDL and is intended for functional verification using Xilinx ISE and ISim simulation tools.

The two-lane accelerator enables two independent operations to be evaluated concurrently, improving the potential processing throughput compared with a single ALU. The modular architecture also provides

flexibility for future extensions and performance evaluation. However, the duplication of ALU units may increase hardware area and active power consumption, while the ripple-carry structure can introduce carry propagation delay. Therefore, the actual benefits in power consumption, area, and timing must be established through synthesis and implementation results. Overall, the project provides a foundation for exploring efficient arithmetic circuit design and parallel processing architectures for FPGA-based systems and future VLSI applications.

IX. FUTURE WORK

The proposed 16-bit ALU with an XNOR-oriented full adder and a two-lane hardware accelerator can be further improved in several ways. The architecture can be extended to 32-bit and 64-bit datapaths to support more complex computational requirements. Faster adder architectures, such as carry-lookahead, carry-select, carry-skip, and prefix adders, can be incorporated to reduce carry propagation delay and improve arithmetic performance.

The accelerator can be extended to four or eight parallel ALU lanes to support higher levels of parallel processing. Pipelining can also be introduced to improve operating frequency and processing throughput. Furthermore, operand isolation and other power-management techniques can be investigated to reduce unnecessary switching activity when particular processing lanes are inactive.

Future research can focus on implementing the proposed full-adder circuit at the transistor level using CMOS or other low-power logic styles. SPICE simulation and physical layout analysis can be performed to compare transistor count, power consumption, propagation delay, and area. Finally, FPGA synthesis and implementation results can be compared under consistent device and operating conditions to determine the actual advantages and limitations of the proposed architecture. These improvements can help develop more scalable and energy-efficient arithmetic units for embedded systems, digital signal processing, and advanced VLSI applications.

X. REFERENCES

[1] N. Venu, A. Engli, S. Rani, and M. K. Ananthula, “Low Power Area Efficient ALU with Low Power Full Adder,” International Journal for Innovative Engineering and Management Research, vol. 11, Special Issue 06, pp. 167–170, July 2022. [Online]. Available: Download paper.

[2] D. Anitha, K. Manjunatha Chari, and P. Satish Kumar, “Low Power ALU Design Considering PVT Variations,” International Journal of Computer Applications, vol. 104, no. 17, pp. 19–23, October 2014. doi: 10.5120/18300-9442.

[3] D. Kumar and M. Kumar, “Implementation of Parallel Computing and Adiabatic Logic in Full Adder Design for Ultra-Low-Power Applications,” SN Applied Sciences, vol. 2, article 1388, 2020. doi: 10.1007/s42452-020-3188-z.

[4] K. Sanapala and R. Sakthivel, “Ultra-Low-Voltage GDI-Based Hybrid Full Adder Design for Area and Energy-Efficient Computing Systems,” IET Circuits, Devices & Systems, vol. 13, no. 4, pp. 465–470, 2019. doi: 10.1049/iet-cds.2018.5559.

[5] E. Ramakrishna Reddy, V. Nallathambi, and S. Asaithambi, “A Low-Power High-Speed Full Adder Cell Using Carbon Nanotube Field Effect Transistors,” Indonesian Journal of Electrical Engineering and Computer Science, vol. 31, no. 1, pp. 134–142, July 2023.

[6] A. Anitha and S. Rooban, “A Novel ALU Architecture Implementation Using a Sub-Threshold Adiabatic Logic Design for Low-

Power Processors," IETE Journal of Research, vol. 71, no. 12, pp. 4136–4152, 2025. doi: 10.1080/03772063.2025.2546580.
[7] Y. Penchalaiah, N. V. S. Sravani, S. Vamsi, N. Yaswanth, and V. S., "An Efficient ALU Architecture for Low Power IoT Applications," International Journal for Research in Applied Science & Engineering Technology, vol. 13, no. III, March 2025.
[8] Xilinx, ISE Design Suite: Synthesis and Simulation Documentation. Xilinx, Inc. Available through the official Xilinx documentation resources.
[9] J. M. Rabaey, A. Chandrakasan, and B. Nikolić, Digital Integrated Circuits: A Design Perspective. 2nd ed., Prentice Hall, 2003.
[10] S. Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis. 2nd ed., Prentice Hall, 2003.