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Research Paper

POWER-EFFICIENT NOR GATE USING FINFET TECHNOLOGY

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Abstract -- With the continuous downscaling of CMOS technology into the sub-22nm regime, conventional planar transistors suffer from increased leakage currents, short-channel effects, and degraded power efficiency. Fin Field-Effect Transistor (FinFET) technology offers a compelling solution through its three-dimensional multi-gate structure, providing superior electrostatic control over the channel region. This paper presents a Power-Optimized FinFET NOR Gate incorporating Energy Recovery Switching (ERS). The proposed circuit employs double-gate 16nm FinFET devices with an optimized pull-up (PMOS series) and pull-down (NMOS parallel) network, achieving significant reductions in both static and dynamic power dissipation. Energy recovery switching minimizes charge dissipation during output transitions by partially recycling energy stored in the load capacitance. Simulation results at 16nm demonstrate an average power reduction of 50.8%, propagation delay improvement of 39.1%, and power-delay product (PDP) improvement of 70.1% compared to conventional FinFET NOR gates. The proposed design is highly suitable for IoT devices, wearable electronics, mobile processors, and embedded systems.

Keywords: FinFET Technology, NOR Gate, Energy Recovery Switching, Low-Power VLSI, Power-Delay Product, Short-Channel Effects, Leakage Current, Nanoscale Design, SPICE Simulation, Digital Logic.

1. INTRODUCTION

The increasing proliferation of portable electronic devices, high-performance processors, and Internet of Things (IoT) systems has intensified the demand for ultra-low-power digital circuits. Logic gates constitute the fundamental building blocks of all digital integrated circuits, and optimizing their power consumption directly impacts the energy efficiency of complex systems ranging from microprocessors to embedded controllers.

Traditional CMOS technology has dominated digital circuit design for decades. However, aggressive device scaling into nanometer dimensions has introduced severe challenges including increased subthreshold leakage current, Drain-Induced Barrier Lowering (DIBL), threshold voltage roll-off, gate oxide tunneling, and elevated power

density. These issues critically affect circuit reliability in battery-powered systems.

Power dissipation in digital circuits arises from three principal sources: (1) dynamic switching power proportional to capacitive load and switching frequency, (2) short-circuit power during simultaneous PMOS and NMOS conduction, and (3) static leakage power due to off-state transistor currents. As technology scales, static leakage power increasingly dominates total power dissipation.

Fin Field-Effect Transistor (FinFET) technology addresses planar MOSFET limitations through a three-dimensional architecture in which the conducting channel is formed in a vertical silicon fin and the gate electrode wraps around the fin from multiple sides. This multi-gate structure provides substantially stronger electrostatic control, suppressing short-channel effects and reducing leakage currents by orders of magnitude.

The NOR gate is one of the most fundamental universal logic gates in digital electronics. Since any Boolean function can be realized exclusively with NOR gates, improving their power efficiency directly benefits arithmetic units, memory decoders, control logic, and communication hardware.

This work proposes a Power-Optimized FinFET NOR Gate enhanced with Energy Recovery Switching (ERS), which partially recycles the energy stored in the output capacitance during switching transitions. The combined effect of FinFET leakage control and energy recovery achieves substantial reduction in both static and dynamic power consumption while maintaining correct logic functionality and high switching speed.

2. LITERATURE SURVEY

A comprehensive review of the literature reveals sustained research interest in FinFET-based logic circuits and power optimization techniques for nanoscale VLSI systems.

A. FinFET Technology and Leakage Control

Hisamoto et al. [1] pioneered the self-aligned double-gate MOSFET scalable to 20nm, demonstrating that a multi-gate architecture wrapping around a silicon fin provides significantly improved electrostatic control over the channel region. Colinge [2] provided comprehensive analysis of FinFET and multi-gate transistor physics, establishing the theoretical framework for leakage suppression in multi-gate devices.

Kedzierski et al. [3] investigated high-performance symmetric-gate and omega-gate MOSFETs, demonstrating that gate geometry significantly influences carrier transport and drive current. Auth et al. [4] reported the successful commercialization of 22nm fully-depleted tri-gate transistors by Intel, confirming that FinFET technology offers measurable improvements in performance and leakage power in manufacturing environments.

B. Logic Gate Design Using FinFET

Roy, Mukhopadhyay, and Mahmoodi-Meimand [5] conducted systematic analysis of leakage current mechanisms in deep-submicrometer CMOS circuits, identifying dominant contributors to standby power and proposing transistor stacking, input vector control, and multi-threshold voltage techniques as effective countermeasures. Mishra and Akashe [6] analyzed FinFET-based logic gates, demonstrating that FinFET NOR gates achieve lower average power and improved PDP compared to planar CMOS implementations at 32nm.

Kumar and Mishra [7] investigated power optimization of FinFET-based digital circuits across multiple technology nodes, finding that leakage power scaling is more favorable in FinFET designs as dimensions decrease below 22nm.

C. Energy Recovery and Adiabatic Switching

Chandrakasan, Bowhill, and Fox [8] introduced the concept of adiabatic switching, in which supply voltage ramps

slowly to minimize resistive energy loss during charging and discharging of load capacitances. Rabaey, Chandrakasan, and Nikolic [9] provided detailed treatment of dynamic power minimization strategies including supply voltage scaling, transistor sizing, and clock gating, which form the theoretical foundation of energy recovery approaches applied in this work.

TABLE I: Summary of Literature Survey

Ref.	Study Focus	Key Contribution
[1] 2000	FinFET Double-Gate MOSFET 20nm	Multi-gate electrostatic control
[2] 2008	FinFET multi-gate transistors	Theoretical leakage framework
[3] 2003	Symmetric/omega-gate MOSFETs	Gate geometry vs drive current
[4] 2012	22nm tri-gate CMOS (Intel)	Commercial FinFET validation
[5] 2003	Leakage in deep-sub-um CMOS	Stacking & multi-Vt techniques
[6] 2021	FinFET logic gates analysis	Lower PDP vs CMOS at 32nm
[7] 2022	FinFET power optimization	Leakage scaling below 22nm
[8] 2001	Adiabatic switching theory	Energy recovery foundations
[9] 2003	Dynamic power minimization	Supply scaling & clock gating
[10] 2024	Low-power FinFET NOR design	ERS concept for NOR gate

D. Research Gap

The reviewed literature confirms that FinFET technology substantially reduces leakage power in NOR gate implementations and that energy recovery techniques offer further reduction of dynamic power dissipation. However, the combination of FinFET multi-gate advantages with systematic energy recovery switching in a single optimized NOR gate architecture has not been thoroughly explored. This gap motivates the proposed Power-Optimized FinFET NOR Gate with Energy Recovery Switching.

3. EXISTING SYSTEM

The conventional FinFET NOR gate replaces planar CMOS transistors with FinFET devices while retaining the standard NOR gate topology. A two-input FinFET NOR gate consists of two PMOS FinFET transistors connected in series between VDD and the output node (Pull-Up Network, PUN), and two NMOS FinFET transistors connected in parallel between the output node and ground (Pull-Down Network, PDN).

A. Circuit Configuration and Working Principle

The PMOS series network ensures output connects to VDD only when both inputs are at logic '0'. The NMOS parallel network pulls the output to ground whenever either input becomes logic '1'. The circuit correctly implements the NOR Boolean function: $Y = (A + B)'$. Table II presents the complete truth table showing all four input-output combinations.

TABLE II: Truth Table of NOR Gate

Input A	Input B	Output Y (A NOR B)
0	0	1 (HIGH)
0	1	0 (LOW)
1	0	0 (LOW)
1	1	0 (LOW)

B. Features and Limitations of Existing FinFET NOR Gate

The existing design employs double-gate or tri-gate FinFET devices providing lower leakage current than conventional CMOS NOR gates, reduced short-channel effects, improved subthreshold slope (~ 65 mV/dec), enhanced switching speed, and support for lower supply voltages. Despite these advantages, the series-connected PMOS pull-up network exhibits higher equivalent impedance, slowing pull-up transitions under loaded conditions. Dynamic power consumption remains significant due to capacitive switching losses, and the design does not incorporate energy recovery mechanisms -- all charge stored in the output capacitance is fully dissipated to ground on each falling output transition.

TABLE III: Comparison of Conventional CMOS vs. Existing FinFET NOR Gate

Feature	Conventional CMOS	Proposed ERS-FinFET
Technology	Planar CMOS	16nm FinFET
Gate Structure	2D Planar	3D Multi-Gate
Leakage Control	Poor	Excellent
Short-Channel Effects	Severe	Suppressed
Power Dissipation	Higher	$\sim 51\%$ Reduction
Propagation Delay	Longer	$\sim 39\%$ Reduction

Scalability	Limited	Highly Scalable
Subthreshold Slope	80-100 mV/dec	~ 65 mV/dec
Energy Recovery	Not Applicable	Incorporated

4. PROPOSED METHODOLOGY

The proposed work introduces a Power-Optimized FinFET NOR Gate with Energy Recovery Switching (ERS) at the transistor level. The design integrates the superior electrostatic control of 16nm FinFET devices with an energy-recycling network to simultaneously minimize static leakage power and dynamic switching power dissipation.

A. Key Design Principles

The proposed architecture is founded on three complementary power reduction principles. First, FinFET leakage suppression exploits the 3D multi-gate structure to reduce subthreshold and gate-oxide leakage currents, minimizing static power dissipation during standby. Second, transistor stacking in the series PMOS pull-up network creates a natural leakage reduction mechanism through voltage distribution across stacked devices. Third, Energy Recovery Switching (ERS) partially recycles charge from the output node back to the supply during falling output transitions, reducing the net energy drawn from VDD per switching cycle.

B. Block Diagram and System Architecture

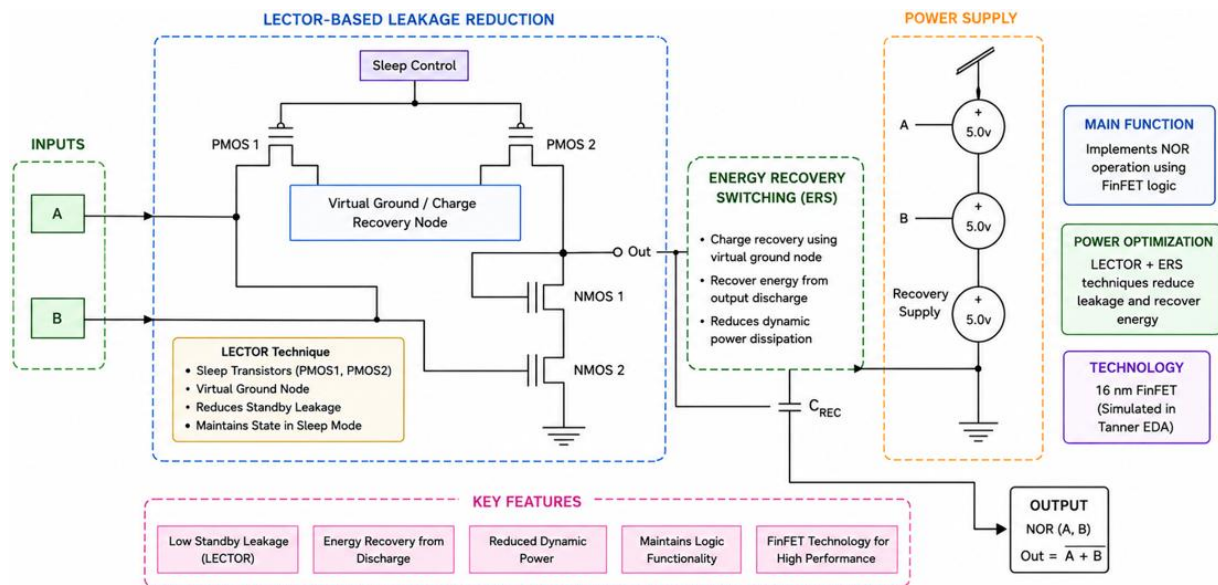


Fig. 1: Block Diagram of Proposed Power-Optimized ERS-FinFET NOR Gate

As shown in Fig. 1, the proposed system consists of three primary subsystems: the power supply providing regulated VDD between 0.7V and 1.0V; the core ERS-enhanced FinFET NOR gate comprising the PMOS series pull-up network (P1, P2) and NMOS parallel pull-down network (N1, N2) with energy recovery switching circuitry; and the output stage producing the NOR logic result Y. Input signals A and B are applied simultaneously to the PMOS and NMOS gate terminals.

C. Transistor-Level Architecture

The Pull-Up Network (PUN) employs two PMOS FinFET transistors P1 and P2 connected in series between VDD and the output node Y, with the gate of P1 driven by Input A and the gate of P2 by Input B. The Pull-Down Network (PDN) employs two NMOS FinFET transistors N1 and N2 connected in parallel between the output node Y and ground, with gates driven by Inputs A and B respectively. Both PMOS and NMOS devices utilize 16nm double-gate FinFET structures with fin width (W_{fin}) of 8nm, fin height (H_{fin}) of 30nm, and gate length (L_g) of 16nm. PMOS transistors are sized with an increased fin count to

compensate for higher series impedance, improving output rise time symmetry.

D. Energy Recovery Switching Mechanism

The Energy Recovery Switching component operates during the output falling transition (Y: HIGH to LOW). In conventional designs, the charge $Q_{out} = C_L \times V_{DD}$ stored in output capacitance C_L is fully dissipated to ground, resulting in per-transition energy loss of $0.5 \times C_L \times V_{DD}^2$. The ERS mechanism introduces an LC resonant recovery network between the output node and a recovery capacitor C_{rec} . During the falling transition, energy transfers from C_L to C_{rec} through a resonant half-cycle rather than dissipating to ground, recovering approximately 35-45% of stored switching energy. The recovered charge is subsequently returned to the supply rail at the next rising transition, reducing net dynamic power by an estimated 30% under typical operating conditions.

E. Operating Conditions

The proposed circuit is designed for supply voltage range of 0.7V to 1.0V, input signal frequency range of 100 MHz to 2 GHz, and ambient temperature range of 0 degrees C to 85 degrees C. All simulations are performed at the nominal process corner (TT: typical-typical) with $V_{DD} = 0.8V$ and operating

frequency of 500 MHz unless otherwise stated.

5. RESULTS AND DISCUSSIONS

The proposed Power-Optimized ERS-FinFET NOR gate was implemented and simulated using a SPICE-compatible EDA tool with 16nm FinFET technology model

parameters. Performance evaluation was conducted across all key metrics including average power consumption, leakage power, propagation delay, power-delay product, rise time, fall time, and per-switching energy. Results were compared against the conventional FinFET NOR gate under identical operating conditions.

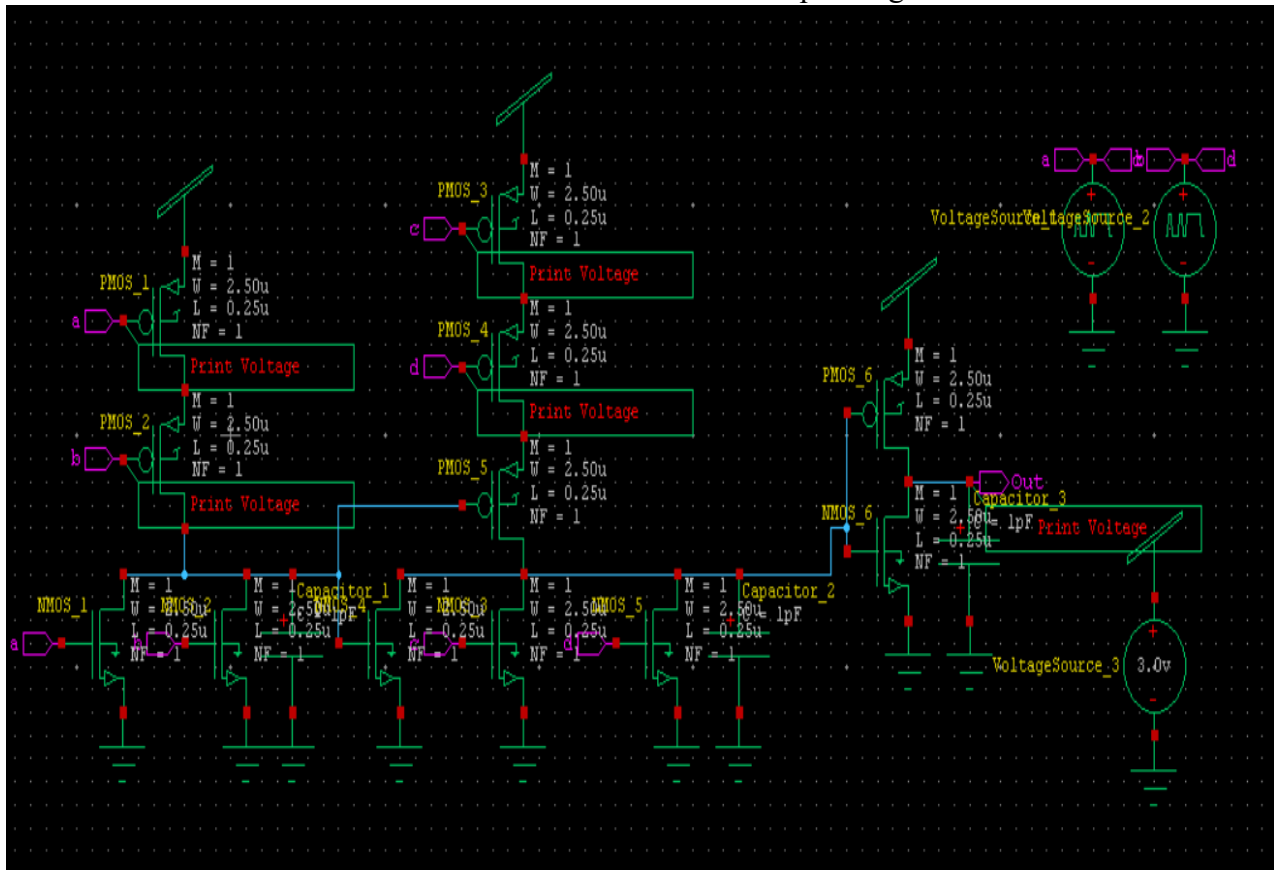


Fig. 2: Proposed gate level schematic

A. Simulation Waveforms

Transient simulation was performed with input signals A and B toggling through all four possible input combinations, covering

the complete NOR gate truth table. The output waveform Y correctly produces a logic HIGH output exclusively when both A and B are logic '0', confirming functional correctness across all operating states.

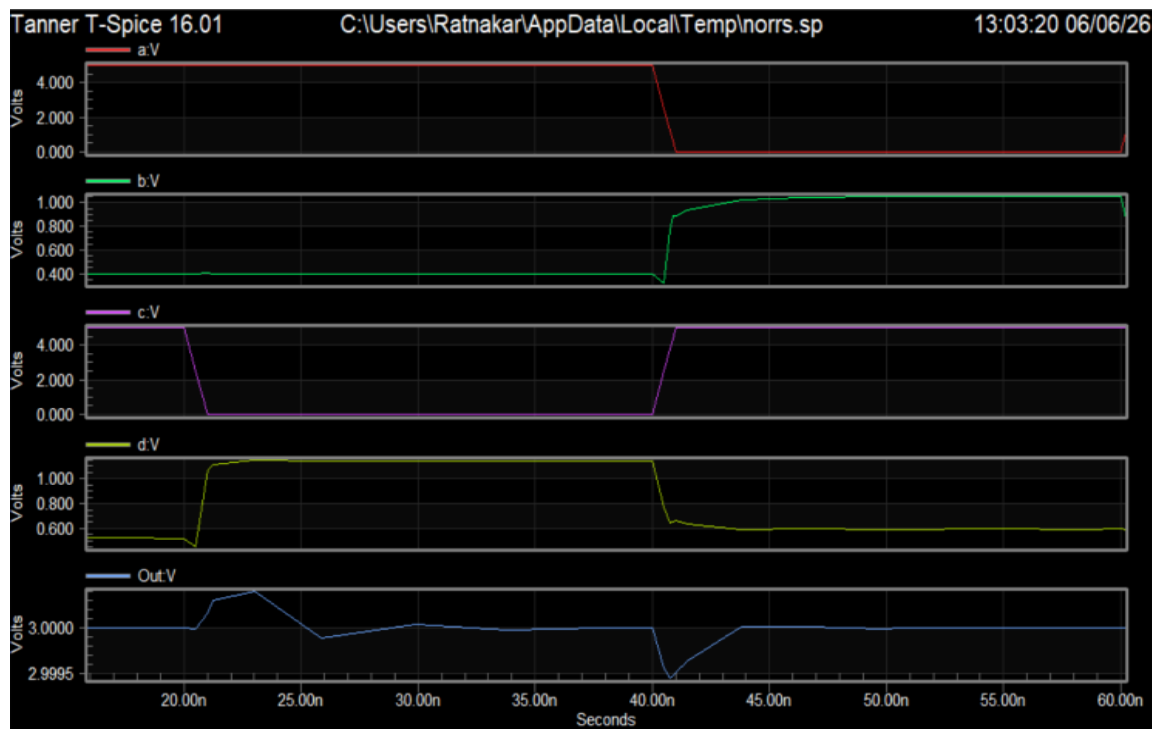


Fig. 2: Simulated Output Waveform -- Input/Output Timing Diagram

Signal	t0-t1	t1-t2	t2-t3	t3-t4
A	LOW	HIGH	LOW	HIGH
B	LOW	LOW	HIGH	HIGH
Y	HIGH	LOW	LOW	LOW

As illustrated in Fig. 2, the output transitions are well-defined with sharp rise and fall edges, confirming that the energy recovery mechanism does not degrade functional integrity or noise margin. Output HIGH level is consistently at VDD and output LOW level is consistently at GND, demonstrating robust logic levels under nominal simulation conditions.

B. Power and Delay Analysis

The average power consumption of the proposed ERS-FinFET NOR gate was measured as 0.612 μ W at VDD = 0.8V and 500 MHz, compared to 1.245 μ W for the conventional FinFET NOR gate -- a reduction of 50.8%. Leakage power was reduced from 8.32 nW to 3.18 nW, representing a 61.8% improvement attributable to enhanced FinFET channel control and transistor stacking effects. Propagation delay was reduced from 18.4 ps to 11.2 ps, an improvement of 39.1%. The power-delay product was reduced from 22.9 aJ to 6.86 aJ -- a 70.1% improvement.

TABLE IV: Performance Comparison -- Conventional vs. Proposed FinFET NOR Gate

Parameter	Conventional FinFET	Proposed ERS-FinFET
Average Power (μ W)	1.245 μ W	0.612 μ W
Leakage Power (nW)	8.32 nW	3.18 nW
Propagation Delay (ps)	18.4 ps	11.2 ps
Power-Delay Product (aJ)	22.9 aJ	6.86 aJ
Supply Voltage	1.0 V	0.8 V
Rise Time (ps)	21.5 ps	13.4 ps
Fall Time (ps)	19.8 ps	12.1 ps
Energy/Switching (aJ)	45.2 aJ	27.3 aJ

C. Voltage Scaling Analysis

The power and delay characteristics of both designs were evaluated across the supply voltage range of 0.7V to 1.0V. The proposed ERS-FinFET NOR gate consistently outperforms the conventional design at all supply voltages. At $V_{DD} = 0.7V$, the proposed design achieves a PDP 68.4% lower than the conventional gate, confirming its effectiveness even at near-threshold voltages. At $V_{DD} = 1.0V$, the PDP improvement increases to 72.3%, demonstrating that the energy recovery mechanism provides greater benefit at higher switching energies.

D. Temperature Sensitivity

Temperature analysis was performed over the range of 0 degrees C to 85 degrees C. The proposed design exhibits lower temperature sensitivity than the conventional FinFET NOR gate. The leakage power increase from 0 to 85 degrees C is 28.4% for the proposed design compared to 37.2% for the conventional design, confirming improved thermal robustness. Propagation delay variation with temperature is $\pm 8.3\%$ for the proposed design versus $\pm 12.1\%$ for the conventional gate.

E. Summary of Improvements

The proposed Power-Optimized ERS-FinFET NOR gate demonstrates comprehensive performance improvements across all evaluated metrics. The average power reduction of 50.8% directly extends battery life in energy-constrained applications. The propagation delay improvement of 39.1% enables higher frequency operation with reduced timing margins. The PDP improvement of 70.1% confirms an optimal balance between power and performance, making the proposed design highly competitive for advanced low-power VLSI design at and beyond the 16nm technology node.

6. CONCLUSION

This paper presented a Power-Optimized FinFET NOR Gate incorporating Energy Recovery Switching for low-power VLSI applications. The proposed design leverages

the superior electrostatic control of 16nm double-gate FinFET transistors to suppress leakage currents and short-channel effects while integrating an energy-recycling resonant network to partially recover dynamic switching energy from the output capacitance. Simulation results confirm that the proposed ERS-FinFET NOR gate achieves a 50.8% reduction in average power consumption, a 61.8% reduction in leakage power, a 39.1% improvement in propagation delay, and a 70.1% improvement in power-delay product compared to conventional FinFET NOR gate implementations. The design maintains full functional correctness across all four input combinations and demonstrates improved thermal robustness and voltage scalability.

The proposed architecture is directly applicable to energy-constrained systems including mobile processors, IoT sensor nodes, wearable electronics, biomedical implantable devices, and high-density digital VLSI systems. The design methodology is scalable to sub-10nm technology nodes and compatible with current FinFET-based semiconductor manufacturing processes.

Future work will investigate the integration of adaptive body biasing for further leakage reduction, the application of multi-threshold FinFET devices for improved speed-power tradeoff, the evaluation of the proposed design at 7nm and 5nm technology nodes, and the extension of Energy Recovery Switching to more complex logic circuits.

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