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Research Paper

DESIGN OF A RECONFIGURABLE APPROXIMATE MULTIPLIER WITH TUNABLE ACCURACY

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ABSTRACT

In CMOS-based application-specific integrated circuit (ASIC) designs, total power consumption is dominated by dynamic power, where dynamic power consists of two major components, namely, switching power and internal power. In this paper, we present a low-power design for an accuracy-controllable multiplier. Multiplication is a key fundamental function for many error-tolerant applications. Approximate multiplication is considered to be an efficient technique for trading off energy against performance and accuracy. This paper proposes an accuracy-controllable multiplier whose final product is generated by a carry-maskable adder. The proposed scheme can dynamically select the length of the carry propagation to satisfy the accuracy requirements flexibly. The partial product tree of the multiplier is approximated by the proposed tree compressor. A multiplier design is implemented by employing the carry maskable adder and the compressor. Compared with a conventional multiplier, the proposed multiplier reduced power consumption. The implementation, synthesis and simulation are executed and noted in the Xilinx-ISE in Verilog HDL language.

1. INTRODUCTION

Numerous advanced applications require power proficiency. Also, these applications are implanted and additionally battery worked. Instances of such applications are Internet of Things (IoT) gadgets. These applications, for example, picture preparing, detecting, acknowledgment, and AI, are inalienably blunder lenient. Because of the way that exact outcomes are not generally needed, almost precise results typically get the job done. In this way, rough figuring [1] is one of the promising procedures for such applications to fulfill the need of low force utilization. Utilizing this method, force can be exchanged for exactness.

MULTIPLICATION

multiplication is an essentially fundamental activity in applications, for example, the ones presented previously. In this way, lessening the expense of duplication benefits the previously mentioned class of utilizations. This venture centers around a rough multiplier. While a few inexact multipliers have been actualized [1, 2, 3, 4, 5], the scope of such applications is restricted in light of the fact that the greater part of the earlier works need exactness adaptability [2, 3]. Thus, dynamic configurability is essential, particularly for the accompanying two reasons.

Multipliers assume a significant part in the present computerized signal preparing and different applications. With progresses in innovation, numerous scientists have attempted and are attempting to plan multipliers which offer both of the accompanying plan targets – fast, low force utilization, consistency of format and henceforth less territory or even mix of them in one multiplier in this way making them reasonable for different high velocity, low force and reduced VLSI execution.

The regular augmentation technique is "add and move" calculation. In equal multipliers number of incomplete items to be added is the principal boundary that decides the exhibition of the multiplier. To diminish the quantity of fractional items to be added, Modified Booth calculation is perhaps the most famous calculations. To accomplish speed enhancements Wallace Tree calculation can be utilized to diminish the quantity of successive adding stages. Further by joining both Modified Booth calculation and Wallace Tree strategy we can see benefit of the two calculations in a single multiplier. Anyway, with expanding parallelism, the measure of movements between the halfway items and moderate entireties to be added will build which may bring about decreased speed, increment in silicon zone because of inconsistency of design and furthermore expanded force utilization because of expansion in interconnect coming about because of complex directing. Then again "sequential equal" multipliers bargain speed to accomplish better execution for territory and force utilization. The determination of an equal or chronic multiplier really relies upon the idea of use. In this talk we present the duplication calculations and design and analyze them as far as speed, territory, force and blend of these measurements.

The basic method of multiplier explains below

```
   123
 x 456
 =====
   738  (this is 123 x 6)
  615   (this is 123 x 5, shifted one position to the left)
+ 492    (this is 123 x 4, shifted two positions to the left)
 =====
 56088
```

The binary multiplication also happens in same way of digit multiplication as shown in below example here by getting partial products and gates are used and we are using adder (half adder ,full adder)adding the columns. An example of 4-bit multiplication method is shown below:

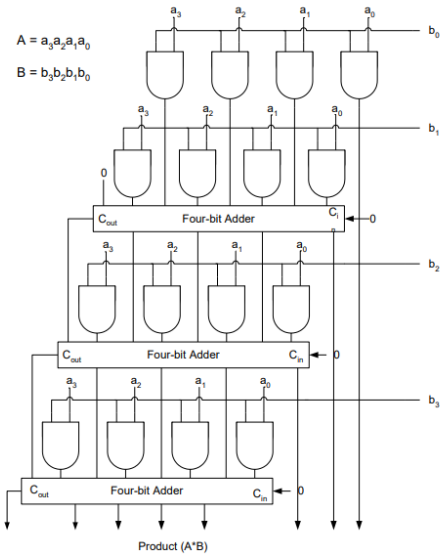


Fig 1.1 multiplication in digital circuits

Albeit the technique is basic as it tends to be seen from this model, the expansion is done sequentially just as in equal. To develop the postponement and region the CRAs are supplanted with Carry Save Adders, in which each convey and entirety signal is passed to the adders of the following stage. End result is gotten in a last viper by any quick snake (typically convey swell viper). In cluster duplication we need to add, however many halfway items as there are multiplier bits. This courses of action are appeared in the figure beneath

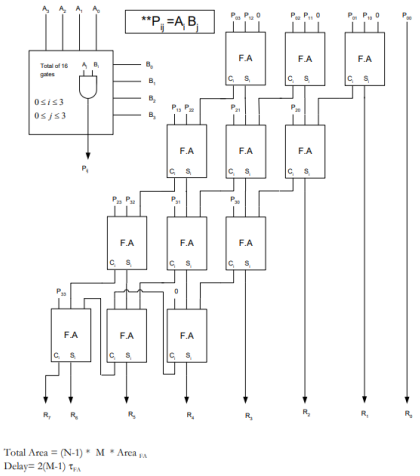


Fig 1.2 Multiplication with Full adder

In applications like mixed media signal handling and information mining which can endure blunder, definite processing units are not generally vital. They can be supplanted with their estimated partners. Exploration on estimated figuring for mistake lenient applications is on the ascent. Adders and multipliers structure the critical segments in these applications. In, estimated full adders are proposed at semiconductor level and they are used in computerized signal preparing applications. Their proposed full adders are utilized in amassing of fractional items in multipliers. To decrease equipment intricacy of multipliers, truncation is broadly utilized in fixed-width multiplier plans. At that point a consistent or variable rectification term is added to make up for the quantization mistake presented by the shortened part. Guess strategies in multipliers center around aggregation of incomplete items, which is pivotal regarding power utilization. Broken cluster multiplier is executed in, where the most un-critical pieces of information sources are shortened, while shaping incomplete items to decrease equipment intricacy. The proposed multiplier in saves not many snake circuits in halfway item amassing. In, two plans of estimated 4-2 blowers are introduced and utilized in halfway item decrease tree of four variations of 8 × 8 Dadda multiplier.

The significant disadvantage of the proposed blowers in is that they give nonzero yield for zero esteemed sources of info, which generally influences the mean relative blunder (MRE) as talked about later. The inexact plan proposed in these brief defeats the current downside. This prompts better accuracy. In static portion multiplier (SSM) proposed in, m-piece fragments are gotten from n-cycle operands dependent on driving 1 bit of the operands. At that point, m × m augmentation is performed rather than n × n increase, where m<n. Fractional item hole (PPP) multiplier in precludes k progressive incomplete items beginning from jth position, where j ∈ [0, n-1] and k ∈ [1, min(n-j, n-1)] of a n-digit multiplier. In , 2 × 2 surmised multiplier dependents on changing a section in the Karnaugh map is proposed and utilized as a structure square to develop 4 × 4 and 8 × 8 multipliers. In , off

base counter plan has been proposed for use in power proficient Wallace tree multiplier.

2. LITERATURE VIEW

A. Momeni, J. Han, P. Montuschi, and F. Lombardi, "Design and Analysis of Approximate Compressors for Multiplication", Inexact (or approximate) computing is an appealing paradigm for virtual processing at nanometric scales. Inexact computing is mainly thrilling for laptop mathematics designs. This paper offers with the analysis and design of two new approximate 4-2 compressors for utilization in a multiplier. These designs rely on distinctive functions of compression, such that imprecision in computation (as measured by means of the error charge and the so-known as normalized blunders distance) can meet with appreciate to circuit-based figures of merit of a layout (wide variety of transistors, postpone and power consumption). Four specific schemes for making use of the proposed approximate compressors are proposed and analyzed for a Dadda multiplier. Extensive simulation results are provided and an application of the approximate multipliers to photograph processing is offered. The results display that the proposed designs accomplish large discounts in electricity dissipation, put off and transistor count number in comparison to a precise layout; furthermore, two of the proposed multiplier designs provide exceptional talents for image multiplication with admire to common normalized mistakes distance and top sign-to noise ratio (more than 50 dB for the taken into consideration photo examples).

C. Liu, J. Han, and F. Lombardi, "A Low-Power, High-Performance Approximate Multiplier with Configurable Partial Error Recovery", Proc. Of IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE), [Approximate circuits were considered for errors-tolerant packages which could tolerate some loss of accuracy with improved performance and power performance. Multipliers are key mathematics circuits in many such programs consisting of digital signal processing (DSP). In this paper, a novel approximate multiplier with a decrease electricity intake and a shorter essential direction than traditional multipliers are proposed for high-overall performance DSP packages. This multiplier leverages a newly-designed approximate adder that limits its carry propagation to the closest pals for immediate partial product accumulation. Different ranges of accuracy may be performed thru a configurable errors restoration by way of the use of distinctive numbers of maximum massive bits (MSBs) for errors discount. The approximate multiplier has a low suggest error distance, i.e., most of the errors are not vast in magnitude. Compared to the Wallace multiplier, a 16-bit approximate multiplier implemented in a 28nm CMOS manner suggests a reduction in postpone and power of 20% and up to 69%, respectively. It is proven that with the aid of utilizing the suitable mistakes recuperation, the proposed approximate multiplier achieves similar processing accuracy as traditional genuine multipliers however with enormous improvements in electricity and performance.

G. Zervakis, et al., "Design-Efficient Approximate Multiplication Circuits Through Partial Product Perforation" Approximate computing has acquired significant interest as a promising approach to decrease strength consumption of inherently error tolerant applications. In this paper, we cognizance on hardware-level approximation by introducing the partial product perforation technique for designing approximate multiplication circuits. We prove in a mathematically rigorous manner that during partial product perforation, the imposed mistakes are bounded and predictable, depending only on the input distribution. Through massive experimental evaluation, we observe the partial product perforation approach on special multiplier architectures and disclose the most excellent structure-perforation configuration pairs for distinct mistakes constraints. We show that, as compared with the respective actual design, the partial product perforation grants discounts of as much as 50% in power consumption, 45% in location, and 35% in vital put off. In addition, the product perforation method is as compared with the contemporary approximation techniques, i.e., truncation, voltage over scaling, and logic approximation, displaying that it outperforms them in phrases of strength dissipation and error.

T. Yang, T. Ukezono, and T. Sato "A Low-Power High-Speed Accuracy-Controllable Approximate Multiplier Design", Multiplication is a key essential function for plenty errors-tolerant programs. Approximate multiplication is taken into consideration to be a green approach for buying and selling off electricity against performance and accuracy. This paper proposes an accuracy-controllable multiplier whose very last product is generated through a convey-maskable adder. The proposed scheme can dynamically pick the period of the convey propagation to meet the accuracy necessities flexibly. The partial product tree of the multiplier is approximated with the aid of the proposed tree compressor. An eight × 8multiplier design is implemented by using the convey maskable adder and the compressor. Compared with a traditional Wallace tree multiplier, the proposed multiplier reduced energy consumption by between forty-seven.3% and 56.2% and important route delay by way of among 29.9% and 60.5%, relying on the specified accuracy. Its silicon place turned into additionally forty-four.6% smaller. In addition, outcomes from a picture processing software demonstrate that the great of the processed photos may be controlled by using the proposed multiplier layout.

2.1 approximate multiply-and-accumulate (MAC)

A. Cilardo, et al., "High-Speed Speculative Multipliers Based on Speculative Carry-Save Tree", Sacrificing genuine calculations to enhance virtual circuit performance is at the foundation of approximate computing. In this paper, an approximate multiply-and-accumulate (MAC) unit is introduced. The MAC

partial product terms are compressed by the usage of easy OR gates as approximate counters; furthermore, to in addition save power, decided on columns of the partial product phrases are not fashioned. A repayment term is added inside the proposed MAC, to lessen the general approximation blunders. A MAC unit, specialized to carry out 2D convolution, is designed following the proposed technique and applied in TSMC 40nm technology in 4 one-of-a-kind configurations. The proposed circuits reap electricity financial savings greater than 60%, as compared to traditional, specific MAC, with tolerable image nice degradation.

J. Liang, et al., "New Metrics for The Reliability of Approximate and Probabilistic Adders", Approximate/inexact computing has turn out to be an attractive method for designing high performance and low energy arithmetic circuits. Floating-factor (FLP) arithmetic is required in many applications, consisting of digital signal processing, picture processing and device mastering. Approximate FLP multipliers with variable accuracy are proposed in this paper; the accuracy and the circuit requirements of those designs are analyzed and assessed according to special metrics. It is shown that the proposed approximate FLP multiplier designs in addition lessen delay, area, strength intake and energy-put off product (PDP) even as incurring approximately 1/2 of the normalized suggest errors distance (NMED) in comparison with the preceding designs. The proposed IFLPM24–15 is the maximum green design when thinking about both PDP and NMED. Case studies with 3 errors-tolerant applications show the validity of the proposed approximate designs.

3. EXISTING METHOD

A typical multiplier consists of three parts: (i) partial product generation using an AND gate; (ii) PPR using an adder tree; and (iii) addition to produce the final result use a CPA. Power consumption and circuit complexity are dominated by the PPR [6], and the multiplier's critical path is dominated by the propagated carry chain in the CPA [5].

3.1 Approximate Tree Compressor

Figure 1(a) shows an accurate half adder, for which the following equation can be obtained:

$$\{c, s\} = a + b = 2c + s = (c + s) + c,$$

where {,} and + denote concatenation and addition, respectively. The value c is generated by a AND b and s is generated by a XOR b, so (c+ s) can be generated by a OR b. Based on the above, consider the basic logic cell shown in Fig. 1(b), for which the following equations can be obtained:

$$p = c + s,$$
$$q = c,$$
$$\{c, s\} = a + b = p + q.$$

This is called an incomplete adder cell (iCAC). Table I shows the truth tables for an accurate half adder and an iCAC. Note that the bit position of c and that of s, p, and q are different. As can be seen, q is equal to c. While p is not equal to s, the precise sum can be obtained by adding p and q, so the iCAC is not an approximate adder but an element of a precise adder.

By extending the above equation to m bits, the following equation can be obtained:

$$S = A + B = P + Q.$$

where A, B, P, and Q are m -bit values, the bits of which correspond to a, b, p, and q, respectively. A row of eight iCACs, used for 8-bit inputs, is shown in Fig. 2.

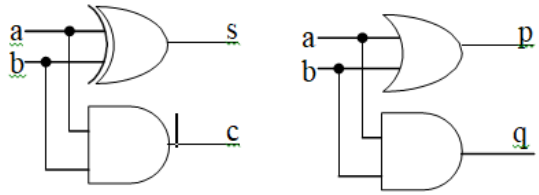
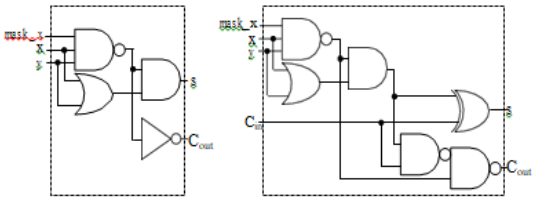


Fig 3.1accurate incomplete adder

Inputs		Outputs			
		Accurate half adder		Icac	
a	b	C	S	Q	P
0	0	0	0	0	0
0	1	0	1	0	1
1	0	0	1	0	1
1	1	1	0	1	1

4.2 Carry-maskable Adder

A CMA is implemented to control the accuracy flexibly and dynamically. A k-bit CMA comprises (k −1) carry-maskable full adders and one carry-maskable half adder, and its structure is similar to k bit CPA.



(a) (b)

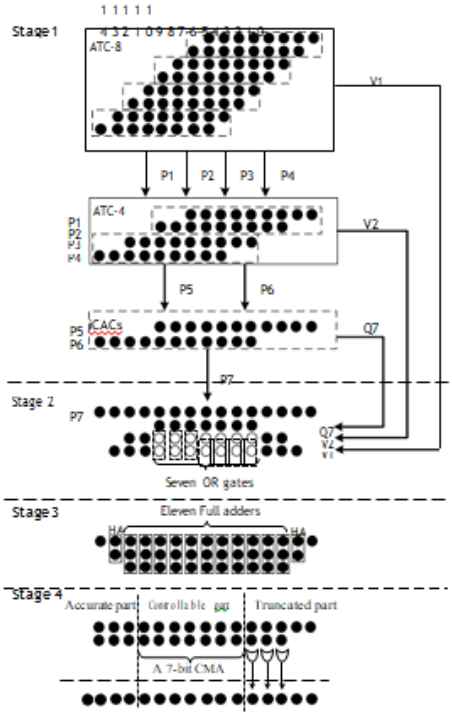


Fig4. 3 existing 8-bit multiplier

4.3 Drawbacks

- Large power consumption
- Circuit Area is more

4. PROPOSED METHOD

4.1 Introduction:

Multiplication in a compressor-based multiplier is processed in three steps. First, the partial products are generated; second, the partial products are reduced; third, the sum of the reduced partial products is generated by a carry propagation adder (CPA). In the implemented multiplier, approximation and configuration are handled in the second and the third steps. These steps are explained in Fig. 6.1.1 and are described in the following subsections.

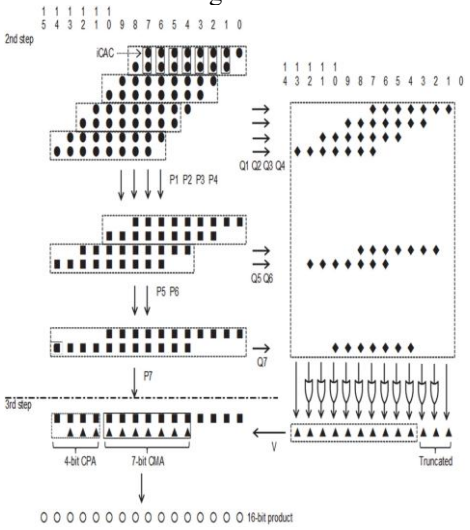
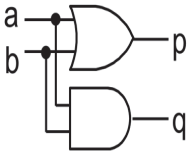


Fig 4.1 Multiplication Flow

4.2 ATC:

Figure 3.1.1 shows the implemented 8-bit approximate multiplier, which has 8 × 8 partial products. In the first step, a logical AND gate operates on a 1-bit multiplicand and a 1-bit multiplier on the same bit position and generates a 1-bit partial product, which is represented by a black circle. In the second step, the ATC [3] is utilized to compress the height of the partial product array and reduce the partial products.

An ATC consists of incomplete adder cells (iCACs) [3]. iCAC is shown in Fig. 4.2.1. In a half adder, the sum s and the carry c of two inputs a and b are expressed as {c, s} =a + b, where {, } and the + sign denote concatenation and addition, respectively. It is obvious from the truth table that p+ q = a + b, where p and q are outputs of iCAC. Hence, {c, s} =p + q and thus the iCAC can generate a precise sum. Consider an n-bit addition of S = A + B where S= {si|i = n — 1, … 0} , A= {ai|i = n — 1, … ,0} and B= {bi|i = n — 1, … ,0}. The carry- out from the most significant bit is ignored. Thus, n iCACs generate P and Q from A and B, where P= {pi|i = n — 1, … ,0} and Q = {qi|i = n — 1, … ,0}. The truth table explains that the "1"s are collected from A and B into P and that P is always greater than S. Hence, it can be seen that P is an approximate sum of A and B. On the other hand, Q works as an error recovery vector to generate the precise S from P, because it is obvious that S= P + Q.



a	b	q	p
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	1

Fig 4.2. iCAC[3]

In Fig. 3.1.1, a black circle represents a partial product. The second step, in turn, consists of three rounds of compressions. In the first round, the 8 × 8 partial products are divided into four groups of two rows, each of which is then operated by seven iCACs by which four pairs of P and Q are generated. They are named (P1, Q1), (P2, Q2), (P3, Q3), and (P4, Q4). A square and a diamond in the figure represent p and q, respectively. In the second round, every two rows, (P1, P2) and (P3, P4), are operated by iCACs by which two pairs of P and Q, (P5, Q5) and (P6, Q6), are generated. In the third round, P5 and Q5 are generated from P5 and P6. Now, an intermediate approximate product, P5, is acquired. On the other hand, there are seven recovery vectors: Q1, Q2, Q3, Q4, Q5, Q6, and Q6.

These vectors are condensed into a single accuracy compensation vector, V. Triangles in Fig. 4.1.1 represent V. V determines the accuracy of the approximate multiplier, because its output is generated by summing P5 and V in the third step. In other words, the way to condense the recovery vectors determines the accuracy. For example, if the vectors are summed up, the precise output will be acquired. Remember that the aim of this study is to build a low-power and small-area approximate multiplier. It is desirable that the

circuit to condense the error recovery vectors and to generate the accuracy compensation vector is as simple as possible. Hence, an OR gate is chosen as the circuit because no significant accumulation of errors is not expected. From the truth table in Fig. 6.2.1, it is observed that "0" is biased to Q, whereas "1" is biased to P. Thus, Qn (n = 1, …, 6) are sparse vectors and operating OR on all of them may not cause any serious error. The least significant bits are truncated from V, because they are less important for the accuracy.

4.3 CMA

In the third step, CMA [5] configures the accuracy of the output product. Figure 6.3.1 shows 1-bit CMA. When $\overline{m}\,\overline{a}\,\overline{s}\,\overline{k} = 1$, it works as the conventional full adder. Otherwise, its carry out is masked to prohibit its propagation and its sum works as s = a OR b. It is assumed that Cin is also masked and is equal to 0. Due to the fact that the most significant bits are very important for accuracy, these are summed up using the conventional CPA. In this design, a 4-bit CPA has been selected. In the remaining bit positions, the CMA is utilized to configure accuracy. In this design, a 5-bit CMA has been selected. Varying the width of the mask controls the carry propagation and thus also controls the output accuracy. For example, if the mask width is 4 bits, that is, $\overline{m}\,\overline{a}\,\overline{s}\,\overline{k} = \{1,1,1,0,0,0,0,0\}$, the upper 3 bits of the CMA work as the precise CPA. Finally, the approximate product is generated by summing P5 and V. White circles in Fig. 4.1.1 represent the output.

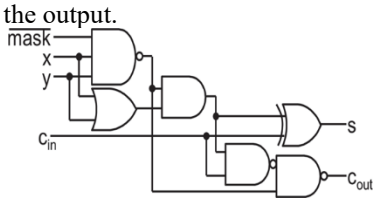


Fig 4.3. CMA[5].

4.4 Advantages:

Proposes a very-low-power and small-area multiplier for accuracy-scalable approximate computing. Implemented approximate multiplier reduces power consumption and circuit area respectively, in the most accurate configuration compared with the Wallace tree multiplier.

In this chapter we discussed about implemented design and its advantage ; in order to overcome the drawback, we are implemented a new model.

5. RESULTS

RTL SCHEMATIC:-

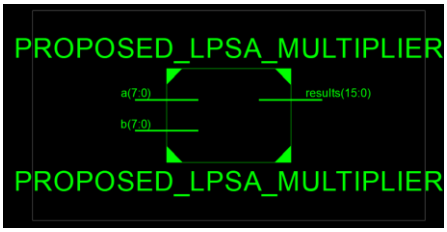


Fig 2.RTL Schematic of The Proposed Design

TECHNOLOGY SCHEMATIC:-

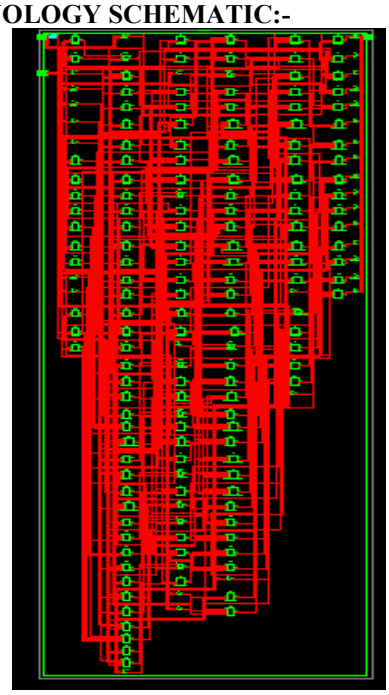


Fig 3 View Technology schematic of existed design

Fig 4.Technology Schematic of The Proposed Design

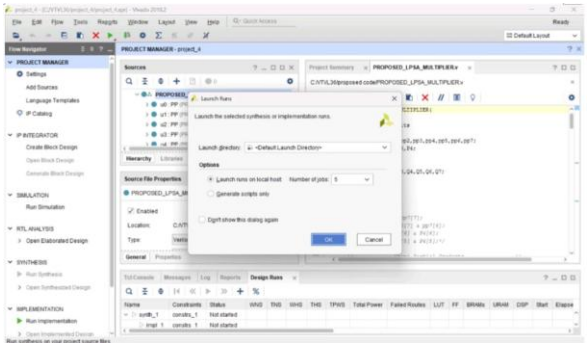


Fig :family selected for synthesis

SIMULATION:-

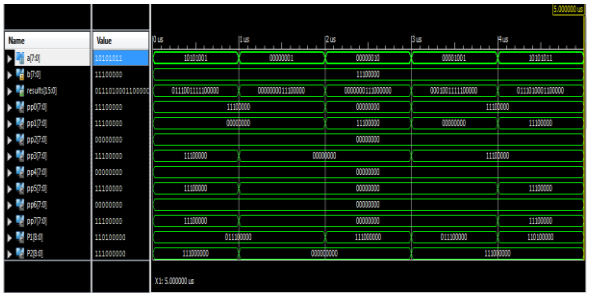


Fig 5:Simaulation wave forms of existed approximate multiplier

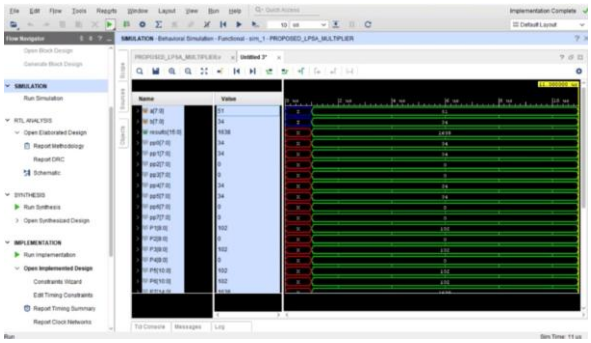


Fig 6:Simaulation wave forms of proposed approximate multiplier

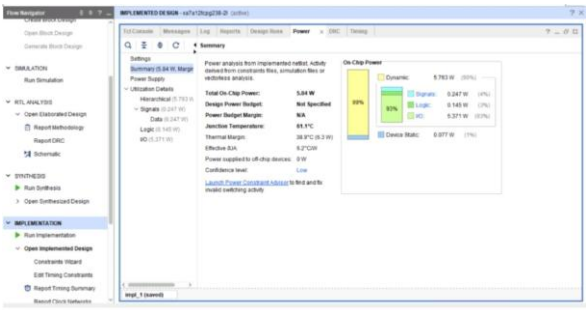


Table :power analyzer

PARAMETERS:-

PARAMETERS	Existed approximate multiplier	Proposed approximate multiplier
NO OF LUT's	133	53
DELAY(ns)	20.376	10.583
POWER(m.Watt)	2.35	0.93

TABLE 2: PARAMETERS TABLE

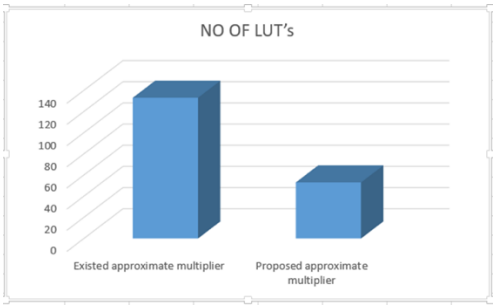


Fig : LUT comparison bar graph

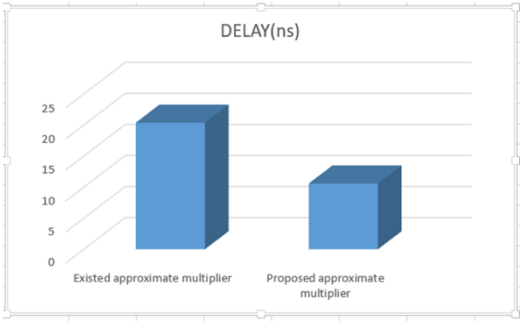


Fig : delay comparison bar graph

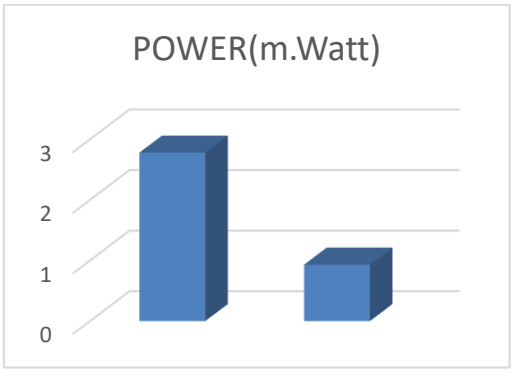


Fig: power comparison bar graph

CONCLUSION

This paper proposes an accuracy-configurable approximate multiplier, which consumes less power than the Wallace tree multiplier and the previously implemented accuracy-scalable multiplier do, respectively. The reduction ratio depends on the required accuracy. In addition, the area of the implemented multiplier is smaller than the area of those multipliers. The lower power and the smaller area are realized by borrowing the concepts of ATC and CMA with careful modifications. At the cost of accuracy, the simple circuit of the basic OR gates are chosen to generate the accuracy compensation vector. This accuracy-configurable approximate multiplier will be beneficial for applications that prioritize power and area rather than accuracy and suffer from fluctuations under working conditions, such as IoT devices.

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