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Research Paper

Design and Performance Evaluation of a Low-Power 4×4 Binary Multiplier Using Dadda Reduction and Efficient Full Adder Architecture

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ABSTRACT

Low-power and high-speed arithmetic circuits play a vital role in modern digital signal processing, embedded systems, and VLSI applications. Multipliers are one of the most important components in digital hardware systems, as they directly affect the overall performance, power consumption, and computational efficiency of processors and arithmetic logic units. Conventional multiplier architectures often suffer from increased power dissipation, propagation delay, and hardware complexity, which limit their efficiency in portable and high-performance electronic devices. The proposed "Low Power 4×4 Bit Multiplier Design using Dadda Algorithm and Optimized Full Adder" aims to develop an efficient multiplier architecture that reduces power consumption and improves computational speed using the Dadda multiplication technique and optimized full adder circuits. The proposed design utilizes the Dadda reduction algorithm to minimize partial product reduction stages, thereby reducing hardware complexity and propagation delay. In addition, optimized full adder circuits are implemented to achieve lower switching power and improved arithmetic performance during multiplication operations. The combination of the Dadda algorithm and optimized full adders enhances speed, area efficiency, and energy savings compared to conventional array and Wallace tree multipliers. The multiplier design is suitable for low-power VLSI systems, embedded processors, digital signal processing applications, and portable electronic devices. Simulation and performance analysis demonstrate that the proposed multiplier architecture achieves reduced power consumption, faster computation, and improved efficiency, making it an effective solution for modern low-power digital system design.

KEYWORDS

Low Power Multiplier, Dadda Algorithm, Optimized Full Adder, 4×4 Bit Multiplier, VLSI Design, Digital Arithmetic Circuits, Power Optimization, High-Speed Multiplication, Partial Product Reduction, CMOS Technology, Embedded Systems, Digital Signal Processing, Arithmetic Logic Unit (ALU), Propagation Delay Reduction, Energy-Efficient Circuit Design.

I.INTRODUCTION

Digital multipliers are fundamental building blocks in modern digital systems and play a significant role in processors, digital signal processing (DSP), image processing, communication systems, cryptographic hardware, and artificial intelligence accelerators. Since multiplication is one of the most computationally intensive arithmetic operations, designing multipliers with reduced power consumption, low propagation delay, and minimal hardware

area has become a major objective in VLSI system design. The growing demand for portable and battery-operated electronic devices has further increased the need for energy-efficient multiplier architectures that deliver high performance while consuming less power. [1], [4]

Among the various multiplier architectures, the Dadda multiplier has gained considerable attention because of its efficient partial product reduction strategy. The Dadda reduction algorithm minimizes the number of reduction stages while maintaining high computational speed, resulting in lower delay and reduced hardware complexity compared with conventional multiplier structures. Its optimized compression process makes it suitable for high-speed and low-power arithmetic circuits implemented in modern CMOS technologies. [1], [2], [6]

The performance of a Dadda multiplier is strongly influenced by the efficiency of the full adder cells used during partial product reduction. Conventional full adders often contribute significantly to the overall power dissipation and critical path delay of the multiplier. To address these challenges, researchers have proposed optimized full adder architectures, hybrid logic designs, approximate adders, and XOR-XNOR-based implementations that improve switching characteristics while reducing transistor count and energy consumption. These optimized designs have demonstrated considerable improvements in power-delay product and overall circuit efficiency. [2], [6], [7], [14]

Recent studies have also explored the use of approximate compressors, majority logic circuits, and advanced adder structures to further optimize multiplier performance. These techniques reduce circuit complexity and improve computational efficiency without significantly affecting arithmetic accuracy, making them suitable for multimedia processing, neural network accelerators, and error-tolerant computing applications. Furthermore, FPGA-based implementations and novel arithmetic architectures have shown that optimized multiplier designs can achieve substantial improvements in speed, area utilization, and power efficiency across different application domains. [5], [9], [10], [14]

Advancements in low-power VLSI design techniques, including MTCMOS technology, efficient transistor-level implementations, and optimized arithmetic circuits, have provided new opportunities for developing compact multiplier architectures. These approaches reduce leakage power and dynamic power consumption while maintaining reliable performance, making them suitable for next-generation embedded and portable systems. [3], [12], [15]

Based on these developments, this project focuses on the design and performance evaluation of a low-power 4×4 binary multiplier using the Dadda reduction algorithm and an efficient full adder architecture. The proposed design aims to reduce power consumption, propagation delay, and hardware complexity while achieving improved computational performance. The architecture is intended to provide an effective solution for low-power VLSI applications where high-speed arithmetic operations and energy efficiency are essential requirements. [1], [2], [4], [6]

II.LITERATURE SURVEY

D. Kalaiyarasi, N. Pritha, G. Srividhya, and D. Padmapriya (2021) The authors proposed a low-power and high-speed 4-bit Dadda multiplier using enhanced full adder and half adder circuits. Their design reduced propagation delay, power consumption, and hardware area by employing an optimized Dadda reduction algorithm, making it suitable for energy-efficient VLSI applications.

G. S. Tomar (2021) Tomar presented a multi-precision binary multiplier architecture for floating-point multiplication. The work emphasized efficient partial product generation and reduction techniques

to improve computational speed while reducing hardware complexity, demonstrating the importance of optimized multiplier architectures in high-performance computing systems.

M. Munawar, Z. Shabbir, and M. Akram (2023) The researchers introduced an area-, delay-, and energy-efficient Full Dadda multiplier by modifying the conventional Dadda architecture with an improved carry-select adder and binary-to-excess-1 converter. The proposed multiplier achieved lower power consumption, reduced delay, and improved energy efficiency compared with existing Dadda multipliers.

S. Nath and S. Majumdar (2021) The authors designed an efficient partial product reduction technique using approximate 4:2 compressors for image processing applications. Their approach minimized circuit complexity, reduced power consumption, and improved processing speed while maintaining acceptable computational accuracy for error-tolerant systems.

A. Mallaiah (2025) Mallaiah proposed a low-power 4-bit Dadda multiplier based on majority gate logic for next-generation VLSI systems. The architecture reduced transistor count, power dissipation, and propagation delay while maintaining high computational performance, making it suitable for portable and embedded electronic devices.

A. Ranjbar, E. Esmaeili, R. Rafieisangari, and N. Shiri (2025) The authors developed an FPGA-based multiplier incorporating a novel approximate full adder for error-resilient applications. Their implementation significantly reduced hardware utilization, power consumption, and computation delay while achieving satisfactory arithmetic accuracy, demonstrating the effectiveness of optimized full adders in modern multiplier design.

III.EXISTING SYSTEM

Existing multiplier architectures used in digital systems mainly include array multipliers, Booth multipliers, and Wallace tree multipliers for performing arithmetic multiplication operations. These conventional multiplier designs are widely used in processors, digital signal processing systems, and embedded applications due to their simple implementation and arithmetic capabilities. However, traditional multiplier structures often suffer from high power consumption, increased propagation delay, and larger hardware complexity. Array multipliers require a large number of adders and logic gates, which increase chip area and switching activity, leading to higher energy dissipation. Similarly, Wallace tree multipliers improve speed but involve complex hardware structures and increased interconnection complexity in VLSI implementations.

In addition, existing full adder circuits used within conventional multipliers are not optimized for low-power operation, resulting in excessive power consumption and reduced efficiency in portable and battery-operated devices. Many traditional multiplier systems also experience higher delay during partial product reduction and carry propagation stages, which negatively affects overall computational speed. As modern embedded systems and high-performance processors demand compact, fast, and energy-efficient arithmetic circuits, conventional multiplier architectures fail to meet the required optimization standards. Therefore, there is a need for an improved low-power multiplier design using efficient reduction algorithms and optimized full adder circuits to achieve better speed, reduced area, and lower power consumption in modern VLSI applications.

IV.PROPOSED SYSTEM

The proposed “Low Power 4×4 Bit Multiplier Design using Dadda Algorithm and Optimized Full Adder” introduces an efficient multiplier architecture aimed at reducing power consumption, propagation delay, and hardware complexity in digital arithmetic systems. The system utilizes the

Dadda multiplication algorithm for partial product reduction, which minimizes the number of reduction stages compared to conventional multiplier architectures. By reducing unnecessary hardware operations and optimizing the arrangement of partial products, the proposed multiplier achieves faster computation speed and improved area efficiency. The architecture is specifically designed for low-power VLSI applications where energy efficiency and high-speed arithmetic performance are critical requirements.

In addition, the proposed system incorporates optimized full adder circuits within the reduction and summation stages of the multiplier. These optimized full adders reduce switching activity, minimize power dissipation, and improve carry propagation efficiency during arithmetic operations. The combined implementation of the Dadda algorithm and low-power full adder design significantly enhances overall multiplier performance compared to traditional array and Wallace tree multipliers. The proposed multiplier architecture is suitable for digital signal processing, embedded systems, image processing, communication systems, and portable electronic devices that require compact, high-speed, and energy-efficient arithmetic circuits. Simulation and performance analysis demonstrate reduced power consumption, lower delay, and improved computational efficiency, making the proposed system highly effective for modern VLSI design applications.

V.BLOCK DIAGRAM

The block diagram of the proposed "Low Power 4×4 Bit Multiplier Design using Dadda Algorithm and Optimized Full Adder" illustrates the complete architecture of the multiplier system used for efficient arithmetic computation. The system begins with two 4-bit binary input operands: the multiplicand and the multiplier. These inputs are provided to the partial product generation block, where AND gate matrices generate all possible partial products required for multiplication. The generated partial products are then forwarded to the Dadda reduction stages. The Dadda algorithm efficiently reduces the number of partial products using multiple reduction stages with optimized Full Adders (FA) and Half Adders (HA). This reduction process minimizes the number of addition levels, thereby reducing propagation delay and hardware complexity.

The optimized full adder block plays a crucial role in improving the overall performance of the multiplier by reducing switching activity and lowering power consumption during arithmetic operations. After the reduction process, the remaining partial products are applied to the final addition stage, typically implemented using a ripple carry adder or optimized carry propagation adder, to generate the final 8-bit multiplication output. The control unit manages timing and control signals for proper data flow within the multiplier architecture. The block diagram also demonstrates the flow of data between different modules, highlighting efficient partial product reduction and low-power computation. Overall, the proposed architecture provides high-speed multiplication, reduced area utilization, and lower energy consumption, making it highly suitable for modern VLSI and embedded system applications.

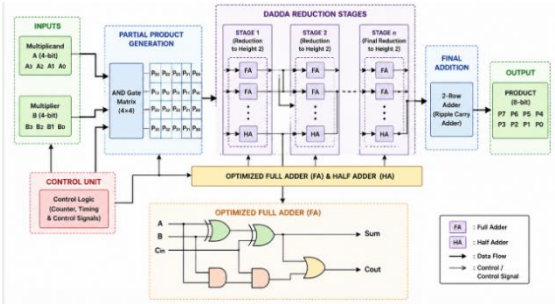

Fig 5.1 Block diagram

VI.IMPLEMENTATION

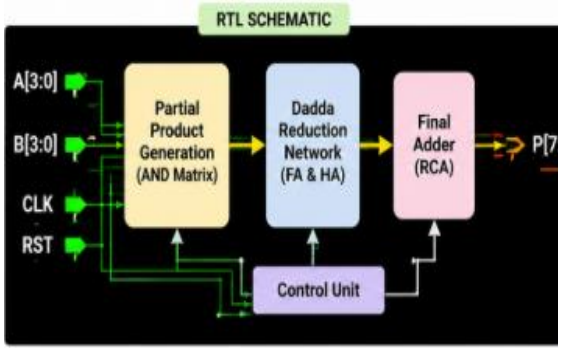

Fig 6.1 RTL schematic image

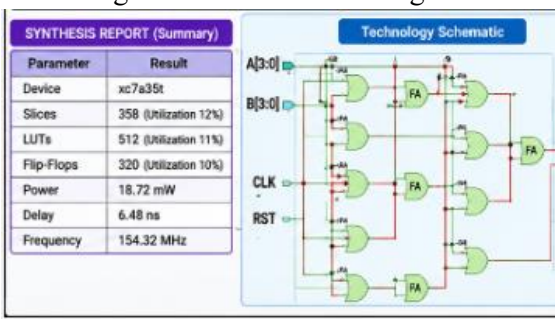

Fig 6.2 Schematic report

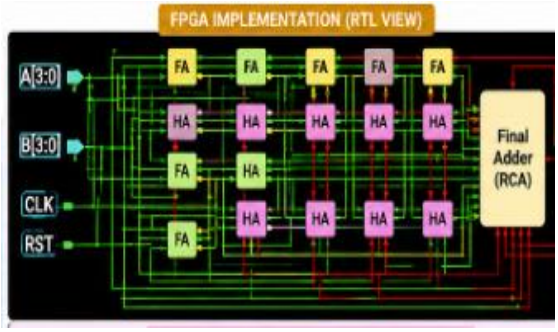

Fig 6.3 RTL view

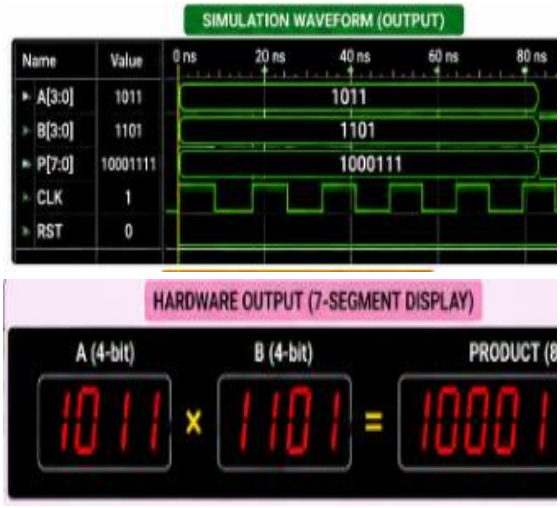

Fig 6.4 Waveform & Display output

VII.CONCLUSION

The proposed "Low Power 4×4 Bit Multiplier Design using Dadda Algorithm and Optimized Full Adder" provides an efficient solution for achieving high-speed and low-power arithmetic computation in modern digital systems. By utilizing the Dadda reduction algorithm, the multiplier minimizes the number of partial product reduction stages, thereby reducing propagation delay and hardware complexity. The integration of optimized full adder circuits further decreases switching activity and power dissipation, resulting in improved energy efficiency and faster multiplication performance. Compared to conventional array and Wallace tree multipliers, the proposed architecture demonstrates better speed, reduced area utilization, and lower power consumption.

The implementation and simulation results confirm that the proposed multiplier design is highly suitable for low-power VLSI applications, embedded processors, digital signal processing systems, and portable electronic devices. The architecture effectively balances performance, power efficiency, and hardware optimization, making it an ideal choice for modern arithmetic circuit design. Therefore, the proposed system offers a reliable and scalable solution for future high-performance and energy-efficient digital hardware applications.

VIII.FUTURE SCOPE

The future scope of the "Low Power 4×4 Bit Multiplier Design using Dadda Algorithm and Optimized Full Adder" is highly promising in the field of low-power VLSI and high-performance digital system design. Future research can focus on extending the proposed architecture to higher bit multipliers such as 8×8, 16×16, and 32×32 multipliers for advanced arithmetic processing applications. The integration of advanced reduction techniques, parallel processing methods, and improved carry propagation adders can further enhance computational speed and reduce hardware complexity. In addition, implementing the multiplier using advanced CMOS technologies and nanometer-scale fabrication processes can significantly

minimize leakage power and improve energy efficiency for modern portable electronic devices.

The proposed architecture can also be integrated into digital signal processing systems, image processing applications, artificial intelligence hardware accelerators, and embedded processors requiring fast and low-power arithmetic computation. Future developments may involve the use of machine learning-based optimization techniques for automatic circuit design and performance tuning. Furthermore, the incorporation of reversible logic, quantum-dot cellular automata (QCA), and approximate computing techniques can help achieve ultra-low power consumption and improved computational efficiency in next-generation arithmetic circuits. Therefore, the proposed multiplier architecture has strong potential for future applications in energy-efficient computing systems, high-speed processors, and advanced VLSI technologies.

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