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Research Paper

DESIGN OF A NANOSCALE CMOS 12-TRANSISTOR MEMORY CELL FOR RELIABLE AEROSPACE SYSTEMS

[1]G. Phanisahithi,[2]M. Aniketh,[3] B. Rahul,[4]N. Manoj Kumar, K. Shashidhar [*]

[1,2,3,4]B. Tech Students, Department of Electronics and Communication Engineering, Samskruti College Of Engineering & Technology

[*] Department of Electronics and Communication Engineering, Samskruti College Of Engineering & Technology

[*]Email:Shashignitc2015@gmail.com

ABSTRACT

The rapid advancement of aerospace electronics and space communication systems has created a strong demand for high-performance memory architectures that provide low power consumption, high stability, radiation tolerance, and reliable operation under extreme environmental conditions. Conventional memory cells used in nanoscale CMOS technology often suffer from challenges such as leakage current, soft errors, process variations, and reduced stability when exposed to harsh aerospace environments including cosmic radiation, temperature fluctuations, and electromagnetic interference. To overcome these limitations, the proposed 12T Memory Cell for Aerospace Applications in Nano Scale CMOS Technology introduces an optimized transistor-based memory architecture capable of achieving enhanced reliability, improved noise margins, and low-power operation suitable for aerospace and satellite systems. The 12-transistor memory cell design improves read and write stability while minimizing leakage power and increasing resistance against radiation-induced faults. The proposed system utilizes nanoscale CMOS fabrication technology to achieve compact area utilization, faster switching speed, and efficient power management for advanced aerospace computing applications. By integrating fault-tolerant design techniques and optimized transistor arrangements, the memory cell provides improved operational stability in extreme environmental conditions. The proposed architecture is highly suitable for aerospace communication systems, avionics, satellite processing units, military electronics, and next-generation space exploration technologies requiring robust and energy-efficient semiconductor memory systems.

Keywords: 12T Memory Cell, Aerospace Electronics, Nano Scale CMOS Technology, Radiation Hardened Memory, Low Power VLSI, SRAM Cell, Semiconductor Memory, Fault Tolerant Design, CMOS Technology, Aerospace Applications, Soft Error Reduction, Leakage Power, VLSI Design, Space Electronics, Nano Electronics.

I. INTRODUCTION

The continuous scaling of complementary metal–oxide–semiconductor (CMOS) technology has enabled the development of compact and energy-efficient memory circuits for modern electronic systems. Static random-access memory (SRAM) is an important component in aerospace processors, satellites, navigation units, and other mission-oriented platforms because of its high operating speed and compatibility with standard CMOS fabrication. However, nanoscale memory cells become increasingly vulnerable to radiation-induced disturbances, leakage current, process variations, and reduced noise margins. These concerns are especially critical in aerospace environments, where energetic particles can disturb the stored information and cause temporary or permanent system failures.

Single-event upset (SEU) is one of the major reliability problems encountered by semiconductor memories operating in radiation-prone environments. A charged particle striking a sensitive storage node may generate a transient current and alter the logical state of the cell. As technology dimensions shrink, the amount of charge required to change the stored value also decreases, making conventional SRAM structures more susceptible to soft errors. To address this issue, researchers have developed hardened memory architectures that improve data

retention without relying entirely on external error-correction mechanisms. A 12-transistor SRAM design capable of recovering from dual-node disturbances demonstrated that structural redundancy can provide improved reliability while maintaining reasonable energy efficiency [1]. Similar work has also shown that radiation-hardened 12T cells can strengthen write capability and support dependable operation in space-oriented systems [2].

The 12T memory architecture has received considerable attention because it offers greater design flexibility for separating read, write, and storage operations. This separation can reduce read disturbance and improve the stability of internal nodes. High-reliability 12T SRAM structures have been investigated specifically for aerospace use, where the memory must continue functioning under radiation exposure and changing operating conditions [3]. Soft-error-hardened 12T designs have also demonstrated the value of carefully arranged feedback paths and redundant storage nodes for protecting stored data in both space and terrestrial applications [4]. These developments indicate that transistor-level circuit design remains an effective approach for improving memory robustness.

Multiple-node upset has become another important challenge as device spacing decreases in nanoscale CMOS technologies. A single radiation event may influence more than one nearby node, limiting the effectiveness of memory cells designed only for single-node recovery. SRAM architectures with multi-node upset recovery have therefore been proposed to provide stronger protection for aerospace electronics [5]. The reliability of emerging nanoscale devices under single-event conditions has also been studied using graphene nanoribbon field-effect transistor SRAM structures, highlighting the broader need to evaluate radiation effects across advanced memory technologies [6]. In addition, radiation-immune SRAM circuits designed for space environments have demonstrated that suitable feedback control and node isolation can significantly reduce soft-error sensitivity [7].

Recent studies have extended SRAM hardening toward multinode upset tolerance and improved operational stability. Soft-error-aware memory cells have been developed to tolerate disturbances affecting several internal nodes while targeting aerospace applications [8]. Other researchers have explored higher-transistor-count structures, such as 16T SRAM cells, to improve read stability and writing capability under radiation effects [9]. Read-speed and stability improvements have also been incorporated into hardened SRAM designs to reduce the performance penalties commonly associated with fault-tolerant circuits [10]. Reliability evaluations focused on single-event upset behavior further emphasize the importance of considering critical charge, sensitive-node response, and recovery capability during memory-cell design [11].

Beyond conventional CMOS SRAM, alternative device structures and mitigation techniques are also being investigated. Junctionless transistor-based memory cells have been examined to understand SEU behavior and possible recovery methods at reduced technology dimensions [12]. More recent hardened architectures, including 18T cells, provide enhanced soft-error resilience through additional redundancy and protected feedback mechanisms [13]. Low-power radiation-hardened SRAM designs have similarly focused on balancing energy consumption with reliable data storage [14]. At the system level, surveys of soft-error mitigation methods show that effective aerospace electronics require coordinated protection strategies across device, circuit, architecture, and system layers [15].

Although increased redundancy can strengthen radiation tolerance, it may also introduce penalties in area, power consumption, and access delay. Therefore, a practical aerospace memory cell must achieve a careful balance among reliability, stability, speed, and hardware overhead. Based on these requirements, this work focuses on the design of a nanoscale CMOS 12-transistor memory cell intended for reliable aerospace systems. The proposed design aims to improve storage stability and resistance to radiation-induced disturbances while maintaining acceptable power and performance characteristics. Such a memory structure can contribute to dependable on-chip storage in satellites, spacecraft electronics, avionics, and other systems operating under demanding environmental conditions.

II. LITERATURE SURVEY

S. Pal, G. Chowdary, and W.-H. Ki (2022) proposed an energy-efficient 12-transistor SRAM cell for low-power aerospace applications. The

design focused on recovering stored information after dual-node upsets caused by radiation. The authors introduced redundant storage paths that allow the affected nodes to restore their original states. The proposed cell achieved a useful balance between soft-error tolerance and energy consumption, making it suitable for dependable aerospace memory systems.

R. Sharma, D. Mondal, and A. P. Shah (2023) developed a radiation-hardened 12T SRAM cell with improved writing capability for space applications. Their architecture used multiple storage nodes and reinforced feedback connections to tolerate single-event upsets. The work mainly addressed the write difficulty commonly observed in hardened memory cells while preserving resistance to radiation-induced faults.

R. Yao et al. (2023) presented a high-reliability 12T radiation-hardened SRAM cell for aerospace environments. The proposed RHB-12T architecture was designed to recover from single-event upsets and selected multi-node disturbances. Simulation using a 28 nm CMOS process showed improved read and write performance compared with several existing hardened SRAM structures. The study demonstrated the suitability of 12T cells for reliable nanoscale aerospace memory design.

P. K. Mukku and R. Lorenzo (2023) introduced a soft-error-hardened 12T SRAM cell for space and terrestrial applications. Their work concentrated on protecting sensitive internal nodes from radiation-induced data changes. The circuit used additional transistors and feedback mechanisms to improve the recovery of stored information after an upset. The design aimed to provide better reliability without excessive hardware overhead.

N. Bai, Y. Zhou, Y. Xu, Y. Wang, and Z. Chen (2023) investigated a highly stable SRAM structure capable of recovering from multi-node upsets. The authors addressed the growing risk of multiple storage nodes being disturbed by a single radiation event in nanoscale technologies. Their design improved soft-error immunity and data recovery capability, making it relevant to aerospace systems operating under harsh radiation conditions.

N. O. Adesina (2023) examined the effect of single-event upsets on SRAM cells based on graphene nanoribbon field-effect transistors. The study analysed the behaviour of advanced nanoscale devices when energetic particles affect sensitive circuit nodes. The work provided useful insights into radiation response, critical charge, and the potential application of emerging transistor technologies in reliable memory systems.

III. EXISTING SYSTEM

In the existing semiconductor memory systems, conventional SRAM architectures such as 6T and 8T memory cells are widely used due to their simple structure and compact area utilization. These memory cells provide acceptable performance for general computing applications but face serious limitations when used in aerospace and high-radiation environments. The major problems associated with traditional memory cells include poor radiation tolerance, increased leakage current, lower static noise margin, and reduced stability during read and write operations.

As CMOS technology scales into nanoscale dimensions, transistor leakage and process variations become increasingly significant. Existing memory systems also experience soft errors caused by high-energy particles and cosmic radiation, which may alter stored data and affect system functionality. In aerospace applications, these faults can lead to mission failures and communication interruptions.

Additionally, conventional memory architectures suffer from high power consumption and reduced reliability when operated under extreme temperature and electromagnetic conditions. Existing systems often require additional error correction hardware, which increases circuit complexity, power consumption, and chip area. Therefore, there is a need for an improved memory architecture capable of providing low-power operation, enhanced stability, and high fault tolerance for aerospace applications.

IV. PROPOSED SYSTEM

The proposed 12T Memory Cell for Aerospace Applications is designed using nanoscale CMOS technology to achieve improved stability, reduced power consumption, and enhanced fault tolerance under harsh environmental conditions. The memory architecture utilizes twelve transistors arranged in an optimized configuration to isolate read and write operations, thereby improving data stability and minimizing operational disturbances.

The proposed system incorporates radiation-tolerant design techniques and low-leakage transistor structures to improve resistance against soft errors caused by cosmic radiation and electromagnetic interference. Separate read and write paths are implemented to enhance operational reliability and reduce data corruption during memory access operations. The memory cell also utilizes optimized transistor sizing techniques to improve static noise margin and reduce leakage power.

Advanced CMOS design methodologies are integrated into the system to achieve compact area utilization and faster switching performance suitable for high-speed aerospace communication and processing systems. The proposed architecture supports low-voltage operation while maintaining stable functionality under temperature variations and radiation exposure.

The memory system is highly suitable for aerospace avionics, satellite communication modules, military electronics, navigation systems, and space exploration devices. By combining low-power operation, enhanced stability, and radiation resistance, the proposed 12T memory architecture provides a reliable solution for modern aerospace electronic systems.

V. Block Diagram

The system architecture of the proposed 12T Memory Cell consists of multiple functional layers including transistor control circuitry, read/write access circuitry, storage nodes, power management modules, and fault tolerance mechanisms. The core memory cell is designed using twelve CMOS transistors arranged to provide independent read and write operations for improved stability and reduced interference.

The write circuitry is responsible for storing data into the memory cell using optimized access transistors and controlled voltage levels. The read circuitry operates independently to retrieve stored data without disturbing the internal storage nodes, thereby improving read stability and minimizing data corruption. The power management layer controls voltage distribution and leakage reduction mechanisms to ensure low-power operation under nanoscale CMOS technology.

The fault tolerance module incorporates radiation-hardening techniques and error-resilient transistor arrangements to protect stored data against radiation-induced soft errors. Advanced isolation structures are implemented to reduce noise coupling and electromagnetic interference within the memory architecture. The monitoring and control unit continuously evaluates memory performance parameters such as static noise margin, leakage current, propagation delay, and switching power consumption.

The overall architecture is optimized to provide reliable operation in aerospace environments while maintaining compact chip area, faster processing speed, and improved energy efficiency suitable for next-generation aerospace electronic systems.

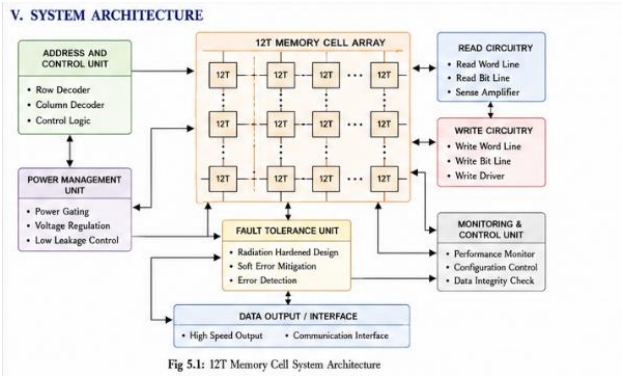

Fig 5.1: 12T Memory Cell System Architecture

VI. IMPLEMENTATION

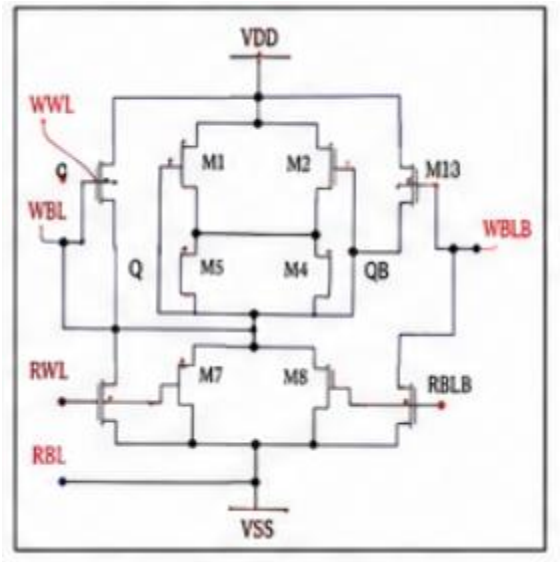

Fig 6.1: CMOS-Based 12T Memory Cell Circuit Design

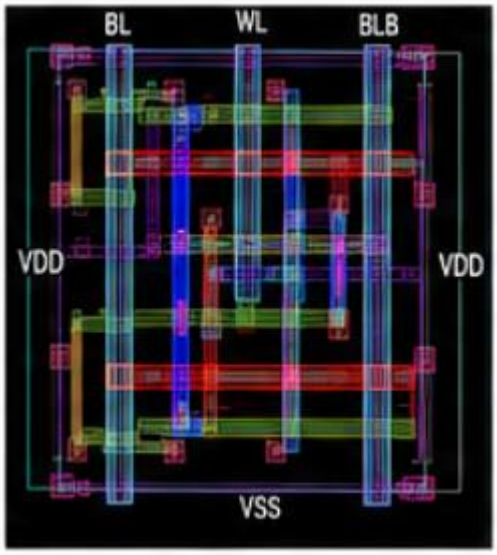

Fig 6.2: Nano Scale Layout Design and Transistor Integration

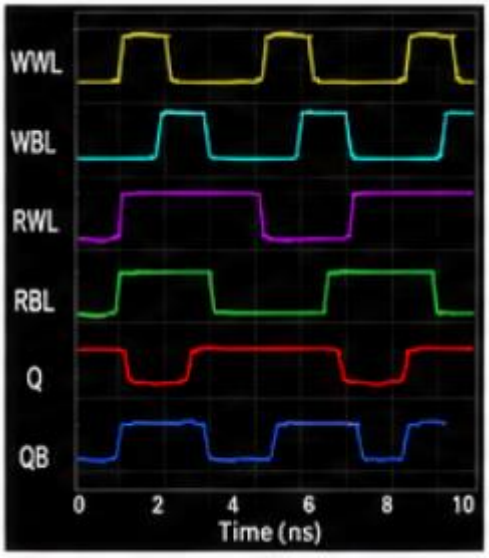

Fig 6.3: Read and Write Stability Simulation Testing

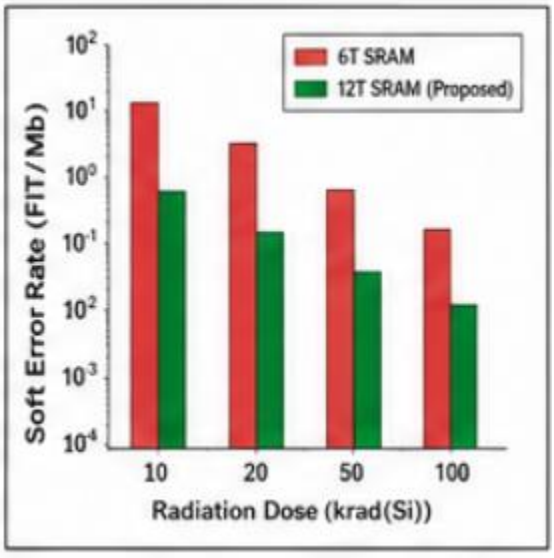

Fig 6.4: Aerospace Radiation Tolerance Performance Analysis

VII. CONCLUSION

The proposed 12T Memory Cell for Aerospace Applications in Nano Scale CMOS Technology provides an efficient and reliable semiconductor memory solution for advanced aerospace electronic systems. By utilizing an optimized twelve-transistor architecture, the proposed memory cell achieves improved read/write stability, reduced leakage current, enhanced static noise margin, and superior radiation tolerance compared to conventional SRAM structures.

The integration of fault-tolerant CMOS design techniques and nanoscale transistor optimization significantly improves operational reliability under harsh environmental conditions such as cosmic radiation, temperature fluctuations, and electromagnetic disturbances. The proposed system supports low-power operation and high-speed memory access suitable for aerospace avionics, satellite systems, and military communication devices. Thus, the proposed memory architecture serves as a robust, scalable, and energy-efficient solution for future aerospace and space computing technologies.

VIII. FUTURE SCOPE

The proposed 12T Memory Cell architecture offers significant opportunities for future research and technological advancements in aerospace semiconductor systems. In the future, Artificial Intelligence and Machine Learning techniques can be integrated with memory management systems to enable adaptive fault detection, predictive error correction, and intelligent power optimization for aerospace computing devices.

Advanced fabrication technologies such as FinFETs, Gate-All-Around FETs, and carbon nanotube transistors can be incorporated to further improve memory density, reduce power consumption, and enhance operational speed. Future research may also focus on integrating quantum-resistant memory architectures and neuromorphic computing systems for next-generation aerospace applications.

The proposed memory system can be extended to support deep-space communication devices, autonomous aerospace systems, and high-performance satellite processing units. Radiation-hardening techniques may be enhanced using advanced shielding structures and error-resilient semiconductor materials to improve long-term

operational reliability in extreme space environments.

Additionally, cloud-integrated aerospace monitoring systems and secure military communication platforms can utilize the proposed memory architecture for high-speed and secure data processing. Future developments in nanoscale CMOS technology and low-power VLSI design will further improve the scalability, efficiency, and intelligence of aerospace memory systems.

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