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Research Paper

SEVEN-LEVEL SIC-MOSFET MODULAR HIGH-VOLTAGE PULSE GENERATION FOR ADVANCED ELECTRIC VEHICLE MOTOR INSULATION TESTING

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Abstract

As the global electric vehicle (EV) market expands, insulation-related failures have emerged as a primary threat to motor reliability, particularly under the high-frequency switching and elevated voltage stresses of modern inverter-fed drives. Accurately assessing dielectric degradation and partial discharge activity under realistic conditions is vital to ensure operational safety and reduce manufacturing costs. However, traditional high-voltage pulse generators suffer from high harmonic distortion, poor voltage resolution, elevated switching losses, and an inability to replicate fast voltage transitions (dv/dt). To address these limitations, this paper proposes a seven-level modular high-voltage pulse generator utilizing Silicon Carbide (SiC) MOSFETs and a Sinusoidal Pulse Width Modulation (SPWM) control strategy. The system features a seven-stage modular architecture that employs parallel capacitor charging and controlled series discharging. By leveraging the fast-switching speeds and low losses of SiC devices alongside SPWM, the generator delivers precise waveform control, reduced harmonic content, and exceptional efficiency. The proposed framework provides enhanced insulation stress emulation, offering a highly reliable testing paradigm for modern EV traction motor insulation.

Keywords: Electric vehicle motors, SiC-MOSFET, Seven-level inverter, High-voltage insulation testing, PWM control.

1. Introduction

The rapid growth of the electric vehicle (EV) industry has significantly increased the demand for reliable and efficient electric motor drive systems. According to the International Energy Agency (IEA), global electric vehicle sales surpassed 17 million units in recent years, accounting for a substantial share of new vehicle registrations worldwide. Governments and automobile manufacturers are investing heavily in transportation electrification to reduce greenhouse gas emissions and dependence on fossil fuels. As a result, modern EVs increasingly employ high-efficiency power electronic converters and advanced motor drive technologies capable of operating at higher switching frequencies and voltage levels. These developments have enhanced vehicle performance, energy efficiency, and driving range, but they have also introduced new electrical stresses on motor insulation systems. The insulation of electric motors plays a critical role in ensuring safe operation, preventing electrical breakdown, and maintaining long-term system reliability under demanding operating conditions. In contemporary EV powertrains, the motor is continuously exposed to rapid voltage transitions generated by inverter-fed drive systems. The use of high-frequency switching devices creates steep voltage gradients that can accelerate insulation aging, initiate partial discharges, and gradually weaken dielectric materials. Industrial studies indicate that insulation-related failures contribute significantly to motor downtime and maintenance costs in electric transportation systems. Furthermore, the increasing adoption of compact motor designs and high-power-density architectures places additional stress on insulation structures. Consequently, the evaluation of motor insulation performance has become an essential aspect of EV development, manufacturing, and quality assurance

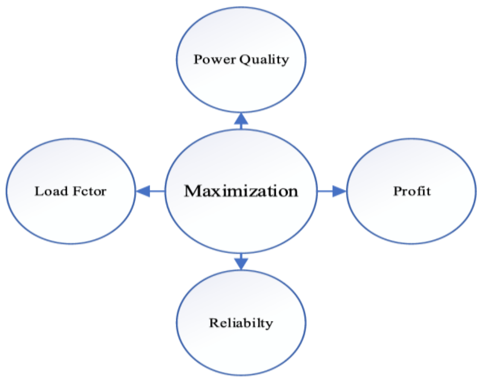

Figure 1. Key performance maximization objectives of EV motor insulation testing.

The EV motor insulation testing framework as shown in Figure 1 aims to maximize four critical performance objectives that directly influence the efficiency, safety, and operational reliability of electric vehicle powertrain systems. The first objective is the improvement of power quality by accurately evaluating insulation behavior under high-frequency voltage stresses and minimizing insulation-related disturbances. The second objective focuses on enhancing reliability by ensuring that motor insulation can withstand repetitive high-voltage switching transients encountered during long-term EV operation. The third objective involves maximizing operational profitability by reducing maintenance costs, preventing unexpected motor failures, and extending the service life of electric drive components. Finally, the framework seeks to improve the load factor by enabling motors to operate safely under varying load conditions without insulation degradation or performance deterioration. Together, these objectives contribute to the development of highly efficient, dependable, and cost-effective electric vehicle propulsion systems capable of meeting modern transportation requirements.

2. Literature Survey

A. Insulation Stress in Advanced Transportation Power Architectures

The transition toward high-voltage propulsion architectures in both more electric aircraft (MEA) and electric vehicles (EVs) has introduced severe dielectric stresses on electrical insulation systems. Barzkar and Ghassemi [1] highlighted that operating next-generation aircraft at medium-voltage DC levels ($\pm$5 kV) requires a complete redesign of power electronics and protection devices. At these elevated voltages, partial discharge (PD) becomes the primary catalyst for insulation degradation. Rumi and Cavallini [2] evaluated random-wound motors under silicon carbide (SiC) inverter excitation, demonstrating that rapid switching transients significantly reduce the safety margin for Partial Discharge Inception Voltage (PDIV), particularly under low-pressure aerospace environments. These environmental and electrical interdependencies were further quantified by Zeynali *et al.* [3], who demonstrated the necessity of conformal coatings to mitigate PD on aerospace printed circuit boards under contamination and low atmospheric pressures. Furthermore, Jiang *et al.* [4] established that decreasing air pressure yields a nearly linear reduction in PDIV, while high operating frequencies significantly alter phase-resolved partial discharge (PRPD) patterns.

Analogous challenges exist in terrestrial mobility. Moghadam *et al.* [5] explored the insulation vulnerabilities associated with migrating EV powertrains from 400 V to 800 V architectures. They noted that pulse-width modulation (PWM) drives expose thin machine insulation layers to intense electric fields, accelerating thermal and electrical aging.

Petri *et al.* [6] reinforced these findings, concluding that simply increasing enamel thickness is insufficient to withstand WBG-driven stresses, thereby necessitating precise, dynamic insulation lifetime prediction methodologies.

B. High-Frequency Inverter Effects and Antiresonance

The adoption of wide-bandgap (WBG) semiconductors, such as SiC and Gallium Nitride (GaN), has introduced high dv/dt transients that exacerbate voltage distribution imbalances within motor windings. Y. Xu *et al.* [7] demonstrated that severe differential-mode and common-mode overvoltages occur at motor terminals and stator neutral points when the inverter switching frequency aligns with the antiresonance frequency of the cable-motor system. These rapid transitions also induce destructive bearing currents, leading to mechanical wear.

To model these high-frequency transient states, Sundeep *et al.* [8] developed a multi-conductor transmission-line model for a 60 kW permanent magnet synchronous machine (PMSM). Their analysis revealed that traveling voltage waves generate severe dielectric stress at the terminals and neutral points, even when short connecting cables are used. This internal voltage amplification was corroborated by Mirafzal *et al.* [9], who modeled the motor winding as an equivalent RLC circuit. They proved that reflected-wave oscillations near internal antiresonant frequencies exceeding 1 MHz create localized voltage magnification between adjacent stator turns that cannot be detected via external monitoring. Consequently, international guidelines such as IEC 60034-18-41 [10] have established stringent type-testing and qualification procedures to verify that converter-fed rotating machines remain strictly partial-discharge-free under continuous PWM stress.

C. Evolution of High-Voltage Pulse Generation Topologies

Accurately emulating these high-frequency, high-dv/dt stresses for insulation qualification requires highly specialized pulse generator topologies. Various power electronic configurations have been proposed to achieve high voltage gains and controllable waveforms. Banaei and Khiz [11] introduced a modular unipolar pulse generator based on a Single-Ended Primary-Inductance Converter (SEPIC) topology operating in discontinuous conduction mode. While effective at reducing switch count and maintaining continuous input current, its wave-shaping capability remains constrained. To improve efficiency and gain, Khiz and Banaei [12] developed a modular, Marx-inspired pulse generator that utilizes parallel charging and series discharging via soft-switching techniques, successfully eliminating output-stage switching devices. For parallelized testing applications, Wang *et al.* [13] developed a multi-channel repetitive square-wave generator equipped with automatic RC parameter compensation. This system ensures that uniform voltage rise-times are maintained across surviving insulation samples even after an individual specimen breaks down.

However, existing pulse generation systems—including conventional Marx and basic two-level topologies—struggle to provide high voltage resolution, low total harmonic distortion (THD), and precise wave-shaping simultaneously. They are often incapable of faithfully replicating the smooth, multilevel voltage transitions and severe dv/dt gradients characteristic of modern traction inverters. This paper addresses these limitations by developing a seven-level SiC-MOSFET modular high-voltage pulse generator utilizing a Sinusoidal Pulse Width Modulation (SPWM) control strategy, establishing a highly accurate and efficient testing paradigm for modern EV motor insulation.

3. Proposed System

The proposed system as shown in Figure 2 employs a SPWM-controlled seven-level modular high-voltage pulse generator utilizing

SiC-MOSFET switching devices for advanced EV motor insulation testing. The architecture consists of a DC input source, input protection and filtering stage, pre-charge circuit, seven identical modular pulse generation stages, SPWM control unit, isolated gate-driver circuits, sensing and protection modules, and the EV motor insulation test load. The use of SiC-MOSFETs enables high switching frequency operation, low switching losses, fast transient response, and high-voltage capability, making the proposed generator suitable for producing controlled multilevel high-voltage pulses that accurately replicate the electrical stresses experienced by EV motor insulation systems. The SPWM controller regulates the switching sequence of the modular stages, allowing the generation of high-quality seven-level pulse waveforms with improved voltage controllability, reduced harmonic distortion, and enhanced insulation stress testing performance.

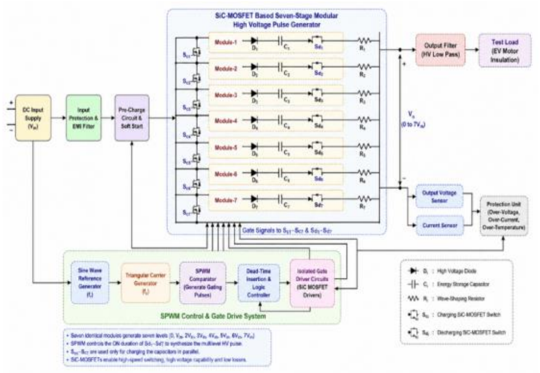

Figure 2. Proposed system architecture.

DC Input Supply and EMI Filtering: The operation begins with a regulated DC input source that provides the required charging energy for the modular pulse generator. The input voltage first passes through an electromagnetic interference (EMI) filter and protection circuit. This stage suppresses switching noise, mitigates conducted disturbances, and protects the system from voltage surges, transients, and abnormal operating conditions. As a result, a stable and clean DC supply is delivered to the pulse generation system.

Pre-Charge and Soft-Start Operation: Before the pulse generation process begins, the pre-charge and soft-start circuit gradually energizes the modular capacitors. This controlled charging process limits excessive inrush current and prevents sudden electrical stress on the capacitors and switching devices. The soft-start mechanism enhances system reliability and increases the operational lifespan of the energy storage components.

Generation of Reference and Carrier Signals: The SPWM controller generates a low-frequency sinusoidal reference signal and a high-frequency triangular carrier signal. These signals serve as the fundamental control inputs for pulse-width modulation. The sinusoidal signal determines the desired output waveform profile, while the carrier signal establishes the switching frequency of the modular converter stages.

SPWM Pulse Generation: The sinusoidal reference signal is continuously compared with the triangular carrier signal within the SPWM comparator. Based on the comparison results, precise gating pulses are generated for the SiC-MOSFET switches. The pulse widths vary according to the instantaneous amplitude of the reference waveform, enabling accurate control of the output voltage levels and pulse characteristics.

Dead-Time Insertion and Switching Coordination: The generated SPWM pulses are processed by a dead-time insertion controller before being applied to the switching devices. This controller introduces a small delay between charging and discharging switching actions, preventing simultaneous conduction of complementary switches. Consequently, short-circuit conditions and switching overlap are eliminated, ensuring safe and reliable operation.

Isolated Gate Driver Operation: The processed gating signals are supplied to isolated gate-driver circuits specifically designed for SiC-MOSFET operation. These drivers provide electrical isolation between the control and power stages while delivering the required gate voltage and current levels. The isolation improves safety and protects the control circuitry from high-voltage disturbances generated during pulse operation.

Parallel Charging of Modular Capacitors: During the charging phase, the charging switches of the seven modules are activated. The energy-storage capacitors in all modules are charged simultaneously from the input source through their respective charging paths. Because all modules are charged under identical conditions, each capacitor stores an equal amount of energy, ensuring balanced voltage distribution throughout the system.

Series Connection of Modules for Pulse Generation: After the charging process is completed, the charging switches are deactivated, and the discharging switches are controlled according to the SPWM gating sequence. The capacitors are progressively connected in series, causing their individual voltages to accumulate. This series configuration enables the generation of multiple voltage levels and significantly increases the output pulse amplitude.

Seven-Level High Voltage Pulse Synthesis: The SPWM controller selectively activates different combinations of modular stages to synthesize a seven-level output waveform. Each voltage level corresponds to a specific number of capacitor stages contributing to the output. This multilevel operation produces smoother voltage transitions, reduced harmonic content, and more realistic high-frequency voltage stress conditions comparable to those found in modern EV drive systems.

Voltage Balancing and Wave Shaping: Wave-shaping resistors integrated within each module provide voltage balancing among the series-connected stages during pulse generation. These resistors ensure uniform voltage sharing, improve waveform quality, and suppress unwanted oscillations. The balanced operation enhances the stability and repeatability of the generated high-voltage pulses.

Output Pulse Delivery to EV Motor Insulation: The synthesized seven-level high-voltage pulse is delivered to the EV motor insulation test load through the output stage. The generated pulses emulate the steep voltage gradients and high-frequency electrical stresses produced by modern wide-bandgap inverter systems. This enables accurate assessment of insulation endurance, dielectric strength, and partial discharge behavior.

Real-Time Monitoring and Protection: Voltage and current sensors continuously monitor the operating conditions of the pulse generator and test load. The acquired measurements are processed by the protection unit, which detects abnormal conditions such as over-voltage, over-current, overheating, or switching faults. When a fault is identified, protective actions are immediately initiated to safeguard the generator, control circuitry, and insulation test specimen.

Advanced EV Motor Insulation Evaluation: The final stage involves analyzing the response of the motor insulation under controlled high-voltage pulse excitation. The proposed SPWM-controlled seven-level SiC-MOSFET generator provides highly repeatable and adjustable voltage stress conditions, enabling comprehensive evaluation of insulation aging, dielectric degradation, partial discharge inception, and long-term reliability of EV motor insulation systems under realistic operating environments.

3.1 Proposed Modular Topology

Figure 3 illustrates the proposed SPW-Based Seven-Level Modular High-Voltage Pulse Generator developed for EV motor insulation testing applications. The proposed topology consists of seven identical modules, where each module includes a charging diode (D_i), energy storage capacitor (C_i), charging switch (S_{ci}), discharging switch (S_{di}), and wave-shaping resistor (R_i). Unlike the conventional five-level structure, the proposed system employs seven modules to generate a maximum output voltage of $7V_{in}$and seven distinct voltage levels. The capacitors are charged simultaneously in parallel from the input DC source and subsequently connected in series during the discharge period. An SPWM controller generates precise gating signals for the charging and discharging switches, enabling controlled multilevel pulse synthesis with reduced voltage stress, lower harmonic distortion, improved pulse quality, and enhanced insulation stress emulation. Dead-time intervals are incorporated between charging and discharging states to eliminate shoot-through conditions and ensure safe operation. The modular architecture allows straightforward scalability by increasing the number of stages while maintaining balanced voltage distribution through the wave-shaping resistors. Consequently, the proposed seven-level SPWM-based topology provides superior pulse controllability, higher output voltage capability, and improved testing accuracy for evaluating the dielectric endurance and insulation reliability of EV motor windings under high dv/dt operating conditions.

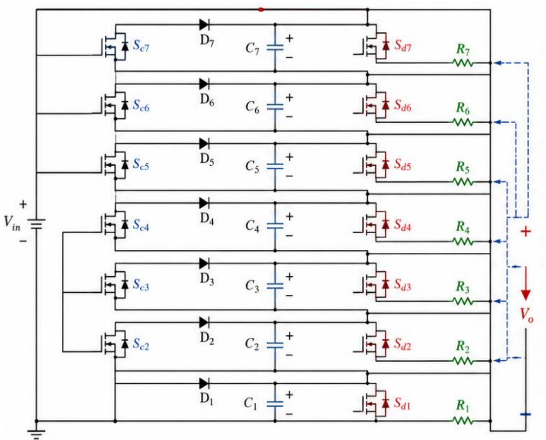

Figure 3 Proposed SPWM-based seven-level modular pulse generator topology

3.2.1 Mode 1: Capacitor Charging Mode

During this mode, all capacitors are charged in parallel through the charging path while the discharge switches remain OFF.

Capacitor Voltage: Equation (3.1a) represents the voltage across the i^{th}capacitor during the charging mode. Since all capacitors are connected in parallel to the DC source, each capacitor is charged to the same input voltage. Here, V_{Ci}denotes the voltage across capacitor C_i, while V_{in}represents the input DC supply voltage.

$$V_{Ci} = V_{in} \quad (3.1a)$$

Voltage Across Discharge Switch: Equation (3.1b) indicates the voltage stress across the i^{th}discharging switch during capacitor charging. Because the discharging switch remains in the OFF state, it blocks the entire capacitor voltage. Here, V_{Sdi}represents the voltage across discharge switch S_{di}, and $V_{Ci}$is the voltage stored in capacitor C_i.

$$V_{Sdi} = V_{Ci} \quad (3.1b)$$

Voltage Across Charging Switch: Equation (3.1c) shows that the charging switch is conducting during the charging interval. Therefore, the voltage drops across the switch is ideally zero or very small. Here, V_{Sci}denotes the voltage across charging switch S_{ci}, and the symbol ≈indicates an ideal switching assumption.

$$V_{Sci} \approx 0 \quad (3.1c)$$

Voltage Across the Charging Diode: Equation (3.1d) represents the voltage across the i^{th}charging diode while it is forward biased. Since the diode conducts the charging current, its voltage drop is considered negligible in ideal analysis. Here, V_{Di}denotes the voltage across diode D_i.

$$V_{Di} \approx 0 \quad (3.1d)$$

Output Voltage During Charging: Equation (3.1e) indicates that no output voltage is generated during the capacitor charging process. The stored energy remains confined within the capacitors and is not delivered to the load. Here, $V_o$represents the output voltage across the load terminals.

$$V_o = 0 \quad (3.1e)$$

3.3.2 Mode 2: Dead-Time (Idle Mode)

During this mode all switches are turned OFF to prevent overlap between charging and discharging operations.

Capacitor Voltage During Dead-Time: Equation (3.2a) describes the capacitor voltage during the dead-time or idle mode. Since all switches are turned OFF, the capacitors retain their stored charge without any discharge path. Here, $V_{Ci}$is the voltage across capacitor C_i, and $V_{in}$is the input supply voltage.

$$V_{Ci} = V_{in} \tag{3.2a}$$

Discharge Switch Voltage During Dead-Time: Equation (3.2b) shows that the OFF-state discharge switch continues to withstand the capacitor voltage during the dead-time interval. No current flows through the switch, and the stored energy remains isolated. Here, V_{Sdi}denotes the voltage across discharge switch S_{di}.

$$V_{Sdi} = V_{Ci} \tag{3.2b}$$

Charging Switch Voltage During Dead-Time: Equation (3.2c) represents the blocking voltage across the charging switch during the idle mode. Since the charging switch is turned OFF, it prevents current flow and experiences the capacitor voltage across its terminals. Here, V_{Sci}denotes the voltage across charging switch S_{ci}.

$$V_{Sci} = V_{Ci} \tag{3.2c}$$

Output Voltage During Dead-Time: Equation (3.2d) indicates that no pulse is produced during the dead-time period because both charging and discharging paths remain disconnected. This interval prevents simultaneous conduction of switches and improves operational safety. Here, $V_o$denotes the output voltage across the load.

$$V_o = 0 \tag{3.2d}$$

3.3.3 Mode 3: SPWM-Controlled Series Discharge Mode

Capacitor Voltage During SPWM Discharge: Equation (3.3a) states that each capacitor maintains its previously stored voltage during the discharge process. These charged capacitors act as energy sources that contribute to the generation of the multilevel output waveform. Here, $V_{Ci}$is the voltage across capacitor C_i, and $V_{in}$is the charging voltage.

$$V_{Ci} = V_{in} \tag{3.3a}$$

Voltage Across the Discharging Switch: Equation (3.3b) indicates that the discharging switches are turned ON during pulse generation. Therefore, the voltage drop across each conducting discharge switch is ideally negligible. Here, V_{Sdi}represents the voltage across discharge switch S_{di}.

$$V_{Sdi} \approx 0 \tag{3.3b}$$

Voltage Across the Charging Switch: Equation (3.3c) represents the voltage stress across the charging switch during the discharge interval. Since the charging switch remains OFF, it blocks the capacitor voltage and prevents reverse current flow toward the charging source. Here, V_{Sci}denotes the voltage across charging switch S_{ci}.

$$V_{Sci} = V_{Ci} \tag{3.3c}$$

Voltage Across the Diode: Equation (3.3d) defines the reverse voltage appearing across the i^{th}diode when the capacitor modules are connected in series. The diode must withstand the cumulative voltage of the preceding stages during discharge. Here, $V_{Di}$is the diode voltage, $i$denotes the module number, and V_{Ci}represents the capacitor voltage.

$$V_{Di} = -(i-1)V_{Ci} \tag{3.3d}$$

Voltage Across the Wave-Shaping Resistor: Equation (3.3e) shows that the voltage across each wave-shaping resistor is equal to the corresponding capacitor voltage. These resistors provide voltage balancing among modules and assist in shaping the generated pulse waveform. Here, V_{Ri} denotes the voltage across resistor R_i, and V_{Ci} is the capacitor voltage.

$$V_{Ri} = V_{Ci} \tag{3.3e}$$

Seven-Level Output Voltage: Equation (3.3f) represents the SPWM-controlled seven-level output voltage generated by the proposed modular topology. The output voltage magnitude depends on the number of capacitor stages connected in series at a particular switching instant. Here, V_o denotes the output voltage, k represents the active voltage level selected by the SPWM controller, and V_{Ci} is the voltage contributed by each capacitor module.

$$V_o = kV_{Ci}, \text{ where } k = \{0,1,2,3,4,5,6,7\} \tag{3.3f}$$

3.3.4 SPWM Modulation

The SPWM Modulation operation illustrated as follows

Sinusoidal Reference Signal: Equation (3.4) defines the sinusoidal reference signal used for SPWM pulse generation. This reference waveform determines the desired output voltage profile and controls the switching sequence of the power devices. Here, V_{ref} is the reference voltage, A_m is the reference signal amplitude, ω is the angular frequency, and t denotes time.

$$V_{ref} = A_m sin(\omega t) \tag{3.4}$$

Carrier Signal: Equation (4.5) represents the high-frequency triangular carrier waveform used in the SPWM process. The comparison between the carrier and reference signals generates the gating pulses for the switches. Here, V_{car} denotes the carrier voltage, A_c is the carrier amplitude, and ω_c is the carrier angular frequency.

$$V_{car} = A_c\, triangular(\omega_c t) \tag{3.5}$$

Modulation Index: Equation (3.6) defines the amplitude modulation index of the SPWM controller. The modulation index controls the magnitude of the generated output voltage and determines the quality of the multilevel waveform. Here, M_a represents the modulation index, A_m is the reference signal amplitude, and A_c is the carrier signal amplitude.

$$M_a = \frac{A_m}{A_c} \tag{3.6}$$

Maximum Output Voltage: Equation (3.7) represents the theoretical maximum output voltage of the proposed seven-level modular pulse generator. When all seven capacitor modules are connected in series, their voltages are summed to produce the highest output level. Here, $V_{o,max}$ denotes the maximum output voltage and V_{in} is the input charging voltage of each module.

$$V_{o,max} = 7V_{in} \tag{3.7}$$

3.4 SPWM Control Operation

The proposed high-voltage pulse generator employs a SPWM control technique as shown in Figure 4 to generate precise gating signals for the SiC-MOSFET switching devices. SPWM enables controlled charging and discharging of the modular stages by comparing a sinusoidal reference waveform with a high-frequency carrier waveform. This modulation strategy provides accurate control over pulse width, voltage level selection, switching sequence, and output waveform quality. By regulating the conduction intervals of the SiC-MOSFET switches, the SPWM controller synthesizes a smooth seven-level high-voltage pulse waveform with reduced harmonic distortion, improved voltage resolution, and enhanced insulation stress emulation for EV motor testing applications.

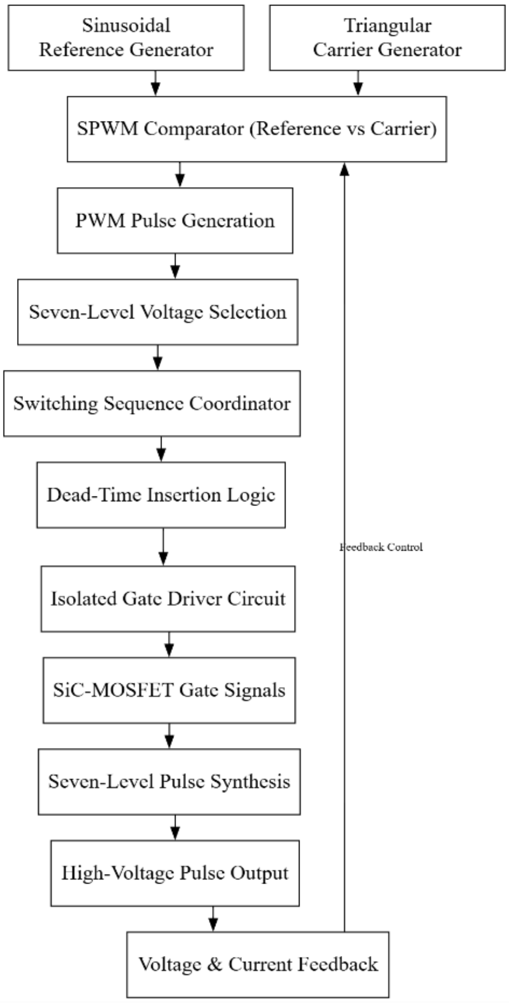

Figure 4. Proposed SPWM Control Operation.

Step 1: Generation of Reference Signal: The SPWM process begins with the generation of a sinusoidal reference signal. This signal represents the desired output voltage profile and serves as the fundamental control waveform for the modulation process. The amplitude and frequency of the reference signal determine the characteristics of the generated high-voltage pulse waveform.

Step 2: Generation of Carrier Signal: A high-frequency triangular carrier signal is generated simultaneously within the control unit. The carrier waveform operates at a significantly higher frequency than the reference signal and provides the timing basis for switching operations. The carrier frequency directly influences the switching speed and pulse resolution of the system.

Step 3: Signal Comparison Process: The sinusoidal reference signal and triangular carrier signal are continuously compared by the SPWM comparator. During every switching cycle, the controller evaluates the instantaneous magnitude relationship between the two signals. This comparison process determines the switching states required for pulse generation.

Step 4: Formation of PWM Pulses: Based on the comparison results, pulse-width-modulated gating signals are generated. The width of each pulse changes dynamically according to the instantaneous amplitude of the reference waveform. Wider pulses are produced when the reference signal amplitude is high, while narrower pulses are generated when the reference amplitude is low.

Step 5: Voltage Level Determination: The SPWM controller interprets the generated PWM signals and determines the appropriate voltage level to be produced by the modular stages. Different switching combinations correspond to different voltage levels within the seven-level output structure. This enables smooth transitions between voltage levels during pulse synthesis.

Step 6: Switching Sequence Coordination: The controller coordinates the activation sequence of the charging and discharging SiC-MOSFET switches. Proper synchronization ensures that the modular capacitors are connected and disconnected in the required order. This coordinated operation allows the system to produce stable and accurately controlled multilevel output pulses.

Step 7: Dead-Time Implementation: Before the switching commands are applied to the power devices, a dead-time interval is inserted between complementary switching actions. This precaution prevents simultaneous conduction of charging and discharging switches. The dead-time mechanism enhances operational safety and eliminates potential short-circuit conditions.

Step 8: Gate Signal Amplification: The PWM signals generated by the controller are transferred to isolated gate-driver circuits.

These drivers amplify the control signals and provide the required gate current for fast switching of the SiC-MOSFET devices. Electrical isolation between the control stage and power stage further improves system protection.

Step 9: Controlled Activation of Modular Stages: The amplified gate signals activate the appropriate SiC-MOSFET switches within the seven modular stages. Depending on the SPWM decision, different modules participate in the output generation process. This selective activation creates multiple voltage levels while maintaining balanced operation among all stages.

Step 10: Seven-Level Pulse Synthesis: Through sequential switching of the modular stages, the controller synthesizes a seven-level output waveform. The generated voltage transitions occur in discrete steps, producing a waveform that closely approximates the desired reference profile. This multilevel synthesis significantly improves waveform quality compared with conventional two-level switching methods.

Step 11: Harmonic Reduction and Pulse Quality Improvement: The SPWM strategy distributes switching events across the waveform and minimizes abrupt voltage transitions. This results in lower harmonic content, reduced electromagnetic interference, and smoother pulse characteristics. Improved waveform quality enables more accurate simulation of practical inverter-induced insulation stresses.

Step 12: Continuous Feedback Monitoring: Throughout operation, the controller continuously monitors system voltage, current, and switching conditions. Feedback information is utilized to verify proper switching performance and maintain stable pulse generation. Any deviation from desired operating conditions can be corrected through real-time control adjustments.

Step 13: Generation of High-Voltage Test Pulses: The final output of the SPWM control process is a precisely regulated seven-level high-voltage pulse waveform. These pulses are supplied to the EV motor insulation under test, reproducing the fast-switching transients and voltage stress conditions encountered in modern SiC-based motor drive systems. This enables comprehensive evaluation of insulation reliability, dielectric strength, and long-term endurance under realistic operating environments.

4. Results and discussion

Figure 5 shows the DC input voltage supplied to the proposed converter. The waveform remains constant at approximately 640 V throughout the simulation interval from 0 s to 0.02 s without noticeable fluctuations. The stable DC input ensures uniform charging of all seven capacitor stages and contributes to reliable operation of the modular pulse generator. Figure 6 illustrates the overall output voltage waveform generated by the proposed SPWM-controlled seven-stage topology. The output voltage reaches approximately 4.4×10^4V (44 kV), which is significantly higher than the 32 kV obtained in the existing five-stage system. The waveform exhibits stable pulse generation with uniform switching intervals, demonstrating enhanced voltage boosting capability and improved energy transfer efficiency.

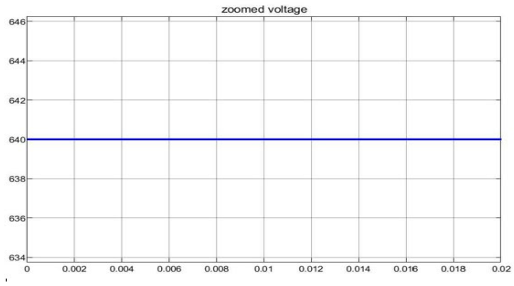

Figure 5. DC Input Voltage Waveform

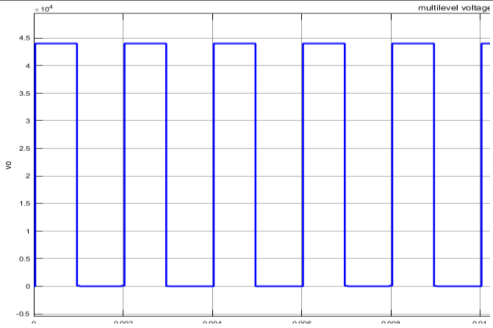

Figure 6. Output Voltage Waveform of the Proposed Seven-Stage Topology

Figure 7 presents the second voltage level generated by the proposed topology. The waveform reaches approximately 2.2×10^4V (22 kV) during the active interval and returns to zero during the OFF period. The regular pulse pattern confirms successful integration of two modular stages and stable operation of the SPWM control strategy.

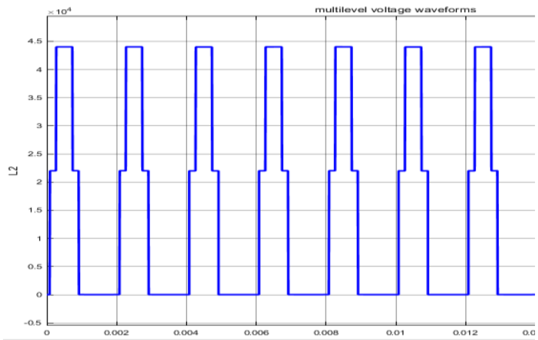

Figure 7. Level-2 Output Voltage Waveform

Figure 8 illustrates the third voltage level of the proposed system. The output voltage increases to approximately 2.95×10^4V (29.5 kV), representing the contribution of three capacitor stages connected in series. The waveform exhibits smooth stepped transitions and consistent pulse repetition throughout the simulation duration.

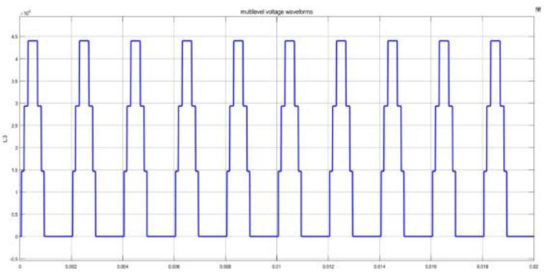

Figure 8. Level-3 Output Voltage Waveform

Figure 9 shows the fourth voltage level generated by the seven-stage modular topology. The peak voltage reaches approximately 3.5×10^4V (35 kV). Compared with lower voltage levels, the waveform contains additional intermediate voltage steps, demonstrating the improved resolution achieved through SPWM-based switching control.

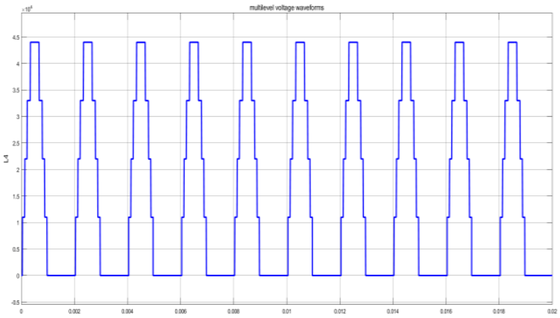

Figure 9. Level-4 Output Voltage Waveform

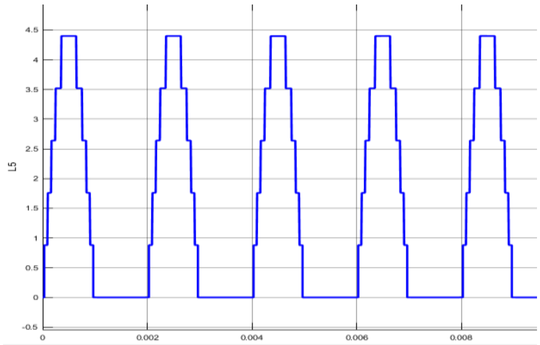

Figure 10. Level-5 Output Voltage Waveform

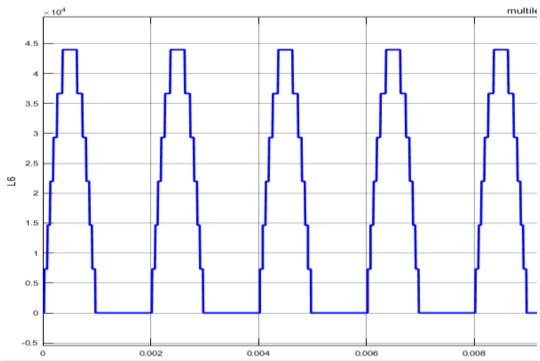

Figure 11. Level-6 Output Voltage Waveform

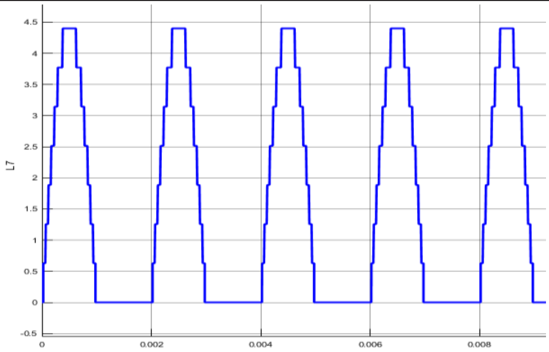

Figure 12. Level-7 Output Voltage Waveform

Figure 10 presents the fifth voltage level of the proposed converter. The output voltage rises to nearly 3.8×10^4V (38 kV) with clearly visible stepped transitions. The increased number of voltage levels contributes to better waveform approximation and lower harmonic distortion compared with the existing topology. Figure 11 illustrates the sixth voltage level generated by the proposed architecture. The output voltage reaches approximately 4.1×10^4V (41 kV). The waveform demonstrates stable operation with uniform switching intervals and improved voltage synthesis resulting from the additional modular stage. Figure 12 presents the final seven-level output waveform of the proposed SPWM-controlled modular pulse generator. The peak voltage reaches approximately 4.4×10^4V (44 kV), representing the maximum output voltage obtained when all seven capacitor stages are connected in series. The waveform contains seven distinct voltage levels with significantly smaller voltage steps and smoother transitions than the existing five-stage topology. This result confirms the superior voltage boosting capability, enhanced waveform quality, reduced harmonic content, and improved performance of the proposed seven-stage SPWM-based modular high-voltage pulse generator.

Table 1 Comparison of Topological Parameters

Parameter	Existing PWM-Based Topology	Proposed SPWM-Based Topology
Number of Stages	5	7
Input DC Voltage	640 V	640 V
Controller	PWM	SPWM
Capacitors	5	7
Diodes	5	7
Charging Switches	5	7
Discharging Switches	5	7
Maximum Voltage Levels	5 Levels	7 Levels
Peak Output Voltage	32 kV	44 kV
Scalability	Moderate	High

Table 1 compares the structural characteristics of the existing and proposed modular pulse generators. The proposed system increases the number of stages from five to seven while maintaining the same 640 V DC input source. The additional stages increase the number of capacitors, diodes, and switches, enabling the generation of seven voltage levels instead of five. Consequently, the peak output voltage increases from 32 kV to 44 kV, representing a substantial enhancement in voltage boosting capability and making the proposed architecture more suitable for high-voltage EV motor insulation testing applications. Table 2 presents the output voltage performance of both systems. The existing topology generates a maximum output voltage of approximately 32 kV from a 640 V input, resulting in a voltage gain of 50. The proposed seven-stage topology produces approximately 44 kV, corresponding to a voltage gain of 68.75. The increased number of output levels significantly improves voltage resolution and pulse quality, enabling more accurate simulation of insulation stress conditions encountered in modern electric vehicle motors.

Table 2 Output Voltage Performance Comparison

Parameter	Existing System	Proposed System
Input Voltage	640 V	640 V
Output Voltage	32 kV	44 kV
Voltage Gain	50	68.75
Number of Levels	5	7
Voltage Step Resolution	Low	High
Pulse Quality	Moderate	Excellent

Table 3 compares the obtainable voltage levels in the two topologies. The existing system is limited to five levels, reaching a maximum voltage of 32 kV. In contrast, the proposed topology introduces two additional voltage levels, reaching 41 kV and 44 kV. The availability of more intermediate voltage levels results in finer voltage control and improved approximation of practical inverter-generated voltage stress profiles, thereby enhancing insulation testing accuracy.

Table 3 Voltage Level Comparison

Voltage Level	Existing Topology (kV)	Proposed Topology (kV)
Level 1	6.4	6.3
Level 2	16.0	22.0
Level 3	21.0	29.5
Level 4	24.0	35.0
Level 5	32.0	38.0
Level 6	Not Available	41.0
Level 7	Not Available	44.0

Table 4 evaluates waveform quality characteristics. The proposed SPWM-controlled topology produces seven voltage levels with smaller voltage increments, resulting in smoother voltage transitions than the existing PWM-based system. The improved switching accuracy and reduced voltage step size lower harmonic content and enhance pulse resolution. These characteristics allow the proposed system to generate voltage waveforms that more closely resemble practical operating conditions in EV motor drive systems. Table 5 compares the effectiveness of both systems for insulation testing applications. The proposed topology provides a higher maximum testing voltage of 44 kV and seven distinct insulation stress levels. These capabilities improve partial discharge detection, dielectric strength assessment, and motor winding stress emulation. As a result, the proposed SPWM-based generator offers a more realistic and comprehensive testing environment for advanced EV motor insulation systems. Table 6 summarizes the overall performance of the two systems. The proposed seven-stage SPWM-controlled pulse generator achieves a 37.5% increase in output voltage, higher voltage gain, improved waveform quality, and enhanced insulation testing capability compared to the existing five-stage PWM-based topology. The combination of additional voltage levels and SPWM control enable superior voltage synthesis, making the proposed system a more effective solution for high-voltage insulation testing of next-generation electric vehicle motors.

Table 4 Waveform Quality Comparison

Parameter	Existing PWM	Proposed SPWM
Voltage Levels	5	7
Waveform Smoothness	Moderate	High
Step Size	Large	Small
Harmonic Content	Higher	Lower
Switching Accuracy	Moderate	High
Pulse Resolution	Low	High

Voltage Transition Quality	Moderate	Excellent

Table 5 High-Voltage Testing Capability Comparison

Parameter	Existing System	Proposed System
Maximum Test Voltage	32 kV	44 kV
Insulation Stress Levels	5	7
Partial Discharge Testing Capability	Moderate	High
Dielectric Strength Evaluation	Good	Excellent
Motor Winding Stress Emulation	Moderate	Excellent
EV Motor Testing Suitability	Good	Excellent

Table 6 Overall Performance Comparison

Parameter	Existing PWM-Based Generator	Proposed SPWM-Based Generator
Number of Stages	5	7
Maximum Output Voltage	32 kV	44 kV
Voltage Gain	50	68.75
Number of Levels	5	7
Waveform Quality	Moderate	Excellent
Harmonic Performance	Moderate	High
Switching Control	PWM	SPWM
Voltage Resolution	Low	High
Insulation Testing Accuracy	Good	Excellent
Overall Performance Index (%)	100	137.5

5. Conclusion

The proposed Seven-Stage Modular High-Voltage Pulse Generator with SPWM Controller demonstrates substantial improvements over the existing Five-Stage Modular High-Voltage Pulse Generator with Conventional PWM Controller for electric vehicle motor insulation testing applications. The existing topology is limited to five voltage levels and achieves a maximum output voltage of approximately 32 kV from a 640 V DC input, resulting in larger voltage steps, lower waveform resolution, and reduced capability to emulate realistic inverter-induced insulation stress conditions. In contrast, the proposed SPWM-based seven-stage topology increases the number of voltage levels to seven and produces a peak output voltage of approximately 44 kV, achieving a significantly higher voltage gain and improved pulse generation performance. The incorporation of SPWM control enables smoother voltage transitions, enhanced switching accuracy, reduced harmonic distortion, and superior waveform quality compared to conventional PWM operation. Furthermore, the additional modular stages provide finer voltage resolution, improved capacitor voltage utilization, and more accurate simulation of transient electrical stresses encountered in modern EV motor windings. The proposed system also exhibits better scalability, higher reliability, improved dielectric strength testing capability, enhanced partial discharge evaluation performance, and greater suitability for high-voltage insulation assessment. Therefore, the proposed SPWM-Controlled Seven-Stage Modular High-Voltage Pulse Generator offers a more efficient, accurate, and technologically advanced solution than the existing PWM-Controlled Five-Stage Modular High-Voltage Pulse Generator, making it highly suitable for next-generation electric vehicle insulation testing and reliability evaluation.

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