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Research Paper

DESIGN AND FPGA IMPLEMENTATION OF A POWER-EFFICIENT VCO-BASED ANALOG-TO-DIGITAL CONVERTER USING CURRENT MODE LOGIC ARCHITECTURE AND FINFET POWER GATING

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Abstract: Analog-to-Digital Converters (ADCs) play a crucial role in modern electronic systems by enabling communication between analog environments and digital processing platforms. Conventional ADC architectures such as Flash, Successive Approximation Register (SAR), Pipeline, and Sigma-Delta ADCs often face challenges related to high power consumption, increased hardware complexity, and limited scalability in advanced semiconductor technologies. To address these limitations, this paper presents a power-efficient Voltage-Controlled Oscillator (VCO)-based Analog-to-Digital Converter utilizing Current Mode Logic (CML) architecture and FinFET-based power gating techniques. The proposed system converts the input analog voltage into a corresponding oscillation frequency using a CML-based VCO, which offers high-speed operation, improved signal integrity, and reduced propagation delay. The generated frequency is processed through an edge detector, digital counter, and output register to produce the final digital output code.

To minimize standby and leakage power consumption, FinFET-based power gating transistors are incorporated into the architecture, enabling efficient power management during inactive operating conditions. The complete design is modeled using Verilog HDL and implemented on an FPGA platform using Xilinx Vivado tools for functional verification and performance evaluation. Experimental analysis demonstrates significant improvements in power efficiency, reduced leakage current, enhanced operating speed, and optimized hardware utilization compared to conventional ADC implementations. The proposed architecture is highly suitable for low-power communication systems, biomedical devices, sensor networks, and Internet of Things (IoT) applications where energy efficiency and high-speed data conversion are critical requirements.

Keywords: Analog-to-Digital Converter (ADC), Voltage-Controlled Oscillator (VCO), Current Mode Logic (CML), FinFET Technology, Power Gating, FPGA

Implementation, Verilog HDL, Low-Power VLSI Design, High-Speed Data Conversion, Internet of Things (IoT), Biomedical Electronics, Xilinx Vivado.

I. INTRODUCTION

The rapid advancement of modern electronic systems has significantly increased the demand for high-speed, low-power, and energy-efficient data conversion techniques. Analog-to-Digital Converters (ADCs) are fundamental building blocks in electronic systems because they serve as an interface between the analog physical world and digital processing systems. Real-world signals such as temperature, pressure, sound, biomedical signals, communication signals, and sensor outputs exist in analog form, whereas modern processors, microcontrollers, and digital communication systems operate using digital data. Consequently, ADCs play a critical role in enabling efficient communication between analog environments and digital platforms.

ADCs are extensively used in wireless communication systems, biomedical instrumentation, automotive electronics, radar systems, image processing applications, sensor networks, industrial automation, and Internet of Things (IoT) devices. The continuous growth of these applications has created a strong need for ADC architectures capable of delivering high conversion speed, low power consumption, reduced hardware complexity, and improved scalability. However, achieving all these objectives simultaneously remains a challenging task for conventional ADC architectures.

Several ADC architectures have been developed over the years, including Flash ADCs, Successive Approximation Register (SAR) ADCs, Pipeline ADCs, and Sigma-Delta ADCs. Flash ADCs offer extremely high conversion speed but require a large number of comparators, resulting in increased power consumption and silicon area. SAR ADCs provide excellent power efficiency and moderate resolution but suffer from limited conversion speed. Pipeline ADCs achieve high throughput and high resolution; however, they require complex calibration circuits and consume considerable power. Sigma-Delta ADCs provide exceptional resolution through oversampling and noise shaping techniques but exhibit lower conversion rates and increased implementation complexity. These limitations motivate the exploration of alternative ADC architectures capable of achieving a better balance among speed, power efficiency, and hardware utilization.

Voltage-Controlled Oscillator (VCO)-based ADCs have emerged as a promising alternative to conventional ADC architectures. Instead of directly converting analog voltage into digital codes using comparator-based quantization, a VCO-based ADC first converts the input voltage into a corresponding oscillation frequency. The generated frequency is then measured using digital counters and converted into digital output data. Since frequency information can be efficiently processed using digital circuits, VCO-based ADCs are highly compatible with modern CMOS technologies and offer improved scalability in advanced semiconductor processes. Their digital-friendly nature

reduces the dependence on complex analog components and enables efficient implementation in low-power integrated systems.

One of the major advantages of VCO-based ADCs is their suitability for advanced deep-submicron technologies. As technology nodes continue to shrink, analog circuit design becomes increasingly challenging due to process variations, noise sensitivity, and reduced voltage headroom. In contrast, VCO-based architectures leverage digital processing techniques that scale more effectively with technology advancements. Consequently, VCO-based ADCs have attracted significant research interest for applications requiring energy-efficient and high-speed data conversion.

To further improve the performance of VCO-based ADCs, Current Mode Logic (CML) has been introduced as an effective high-speed circuit design technique. CML is widely used in high-frequency communication systems because it employs differential signaling and constant current operation. Unlike conventional CMOS logic, which relies on charging and discharging large capacitive loads, CML circuits maintain nearly constant current flow and operate with reduced voltage swings. This characteristic results in lower propagation delay, reduced switching noise, improved signal integrity, and enhanced operating speed.

The differential signaling nature of CML provides excellent immunity against common-mode noise and electromagnetic interference, making it highly suitable for mixed-signal environments. In VCO-based ADC architectures, CML circuits can be utilized to process high-frequency oscillation signals efficiently while maintaining timing accuracy and minimizing jitter. As a result, the integration of CML architecture within the VCO core significantly enhances conversion speed and overall system reliability.

In this work, a power-efficient VCO-based Analog-to-Digital Converter utilizing Current Mode Logic architecture and FinFET-based power gating techniques is proposed. The architecture employs a CML-based Voltage-Controlled Oscillator to achieve high-speed frequency generation and enhanced signal integrity. The oscillation frequency generated by the VCO is processed through an edge detector, frequency counter, and output register to obtain the final digital representation of the analog input signal. FinFET-based power gating transistors are incorporated to minimize leakage power during standby conditions, thereby improving overall energy efficiency.

The proposed design is modeled using Verilog HDL and implemented on an FPGA platform for functional verification and performance evaluation. By combining VCO-based conversion, CML high-speed logic, and FinFET power optimization, the proposed architecture aims to achieve reduced power consumption, lower leakage current, improved operating speed, and efficient hardware utilization. The resulting system is particularly suitable for communication systems, biomedical instruments, sensor networks, portable electronics, and Internet of Things applications where low power operation and high-speed data conversion are essential requirements.

The major contributions of this work include the design of a high-speed VCO-based ADC architecture, integration of Current Mode Logic for improved performance, implementation of FinFET-based power gating for leakage reduction, FPGA-based validation using Verilog HDL, and comprehensive evaluation of power and performance characteristics. The proposed architecture provides a practical and scalable solution for next-generation low-power mixed-signal systems and energy-efficient electronic devices.

II. LITERATURE SURVEY

Analog-to-Digital Converters (ADCs) are essential components in modern electronic systems as they enable the conversion of analog signals into digital data for processing, storage, and communication. With the increasing demand for high-speed communication systems, Internet of Things (IoT) devices, biomedical instruments, and portable electronics, researchers have focused on developing ADC architectures that offer improved speed, reduced power consumption, and efficient hardware utilization. Various ADC architectures have been proposed over the years, each with its own advantages and limitations.

Flash ADCs are among the earliest and fastest ADC architectures. They employ a resistor ladder network and a large array of comparators to perform instantaneous conversion of analog signals. Kester et al. demonstrated that Flash ADCs provide extremely high sampling rates suitable for communication and radar applications. However, the number of comparators required increases exponentially with resolution, leading to significant power consumption and large silicon area. As a result, Flash ADCs become impractical for high-resolution and low-power applications.

Successive Approximation Register (SAR) ADCs have gained considerable attention because of their excellent power efficiency and moderate hardware complexity. Murmann et al. reported that SAR ADCs utilize a binary search algorithm to determine the digital output code, resulting in lower power consumption compared to Flash ADCs. SAR ADCs are widely used in biomedical systems, wireless sensor networks, and battery-powered devices. Nevertheless, their conversion speed is relatively limited because each bit must be resolved sequentially during the conversion process.

Pipeline ADCs have been extensively used in high-speed communication and image-processing systems. Lewis and Gray introduced pipeline architectures capable of achieving high throughput and high resolution simultaneously. The conversion process is divided into multiple stages, allowing parallel operation and increased sampling rates. Despite these advantages, pipeline ADCs require calibration circuits, residue amplifiers, and complex digital correction techniques, which increase power consumption and design complexity.

Sigma-Delta ADCs are well known for providing high-resolution conversion through oversampling and noise-shaping techniques. Candy and Temes demonstrated that Sigma-Delta architectures effectively push quantization noise outside the signal

bandwidth, enabling excellent accuracy and dynamic range. These ADCs are widely employed in audio processing, instrumentation systems, and precision measurement applications. However, their lower conversion speed limits their applicability in high-frequency communication systems.

To overcome the limitations of traditional ADC architectures, researchers have explored Voltage-Controlled Oscillator (VCO)-based ADCs. Straayer and Perrott proposed VCO-based ADCs that convert input voltage into oscillation frequency and subsequently use digital counting mechanisms to generate digital outputs. Since the architecture relies heavily on digital circuits, it exhibits superior scalability and compatibility with advanced CMOS technologies. VCO-based ADCs reduce the need for precision analog components and are particularly attractive for low-power applications.

Recent studies have shown that VCO-based ADCs provide significant advantages in terms of power efficiency and technology scalability.

Daniels et al. investigated time-domain signal processing techniques using VCO-based converters and reported improved energy efficiency compared to conventional voltage-domain ADC architectures. Their work demonstrated that frequency-domain processing can effectively reduce analog circuit complexity while maintaining conversion accuracy.

Current Mode Logic (CML) has emerged as a promising circuit design technique for high-speed applications. Razavi investigated the use of CML circuits in communication systems and demonstrated their ability to achieve low propagation delay, reduced voltage swing, and improved signal integrity. Unlike conventional CMOS logic, CML operates using differential signaling and constant current sources, enabling faster switching speeds and lower timing jitter. These characteristics make CML highly suitable for high-frequency VCO implementations.

Lee et al. further explored CML-based oscillator circuits and reported enhanced operating speed and reduced switching noise compared to traditional CMOS implementations. Their findings revealed that differential architectures improve noise immunity and reduce sensitivity to power supply variations, making them attractive for mixed-signal and high-speed converter systems.

As semiconductor technologies continue to scale into nanometer dimensions, leakage power has become a major challenge. Traditional planar CMOS transistors suffer from significant short-channel effects and increased leakage currents. To address these issues, FinFET technology was introduced as an alternative transistor architecture. Hisamoto et al. pioneered FinFET structures and demonstrated superior electrostatic control over the channel compared to planar MOSFETs. The three-dimensional gate structure significantly reduces leakage current while improving switching performance.

Subsequent research by Auth et al. confirmed that FinFET devices provide lower standby power consumption and better scalability for advanced technology nodes such as 14 nm, 10 nm, and 7 nm processes. Their experimental results indicated substantial reductions in

leakage current and enhanced power efficiency compared to conventional CMOS technologies.

Power gating has become one of the most effective techniques for reducing standby power consumption in low-power integrated circuits. Mutoh et al. proposed sleep transistor-based power gating structures capable of disconnecting inactive circuit blocks from the power supply. Their work demonstrated significant reductions in leakage power during idle operation while maintaining acceptable wake-up performance. Integrating FinFET devices into power gating structures further improves energy efficiency due to the inherently low leakage characteristics of FinFET transistors.

Several researchers have investigated FPGA-based implementation of ADC architectures for rapid prototyping and validation. Xilinx and Altera studies have shown that FPGA platforms provide flexible environments for evaluating digital signal processing architectures and mixed-signal systems. FPGA prototyping enables functional verification, hardware testing, and performance evaluation before ASIC implementation, thereby reducing development time and cost.

Despite significant progress in ADC design, several challenges remain unresolved. Conventional Flash ADCs consume excessive power and area, SAR ADCs suffer from limited conversion speed, Pipeline ADCs require complex calibration, and Sigma-Delta ADCs exhibit lower throughput. Although VCO-based ADCs offer improved scalability and energy efficiency, limited research has been reported on integrating Current Mode Logic architectures with FinFET-based power gating techniques. Furthermore, FPGA-based validation of such integrated architectures remains relatively unexplored.

Therefore, there exists a need for a high-speed, low-power, and area-efficient ADC architecture that combines the advantages of VCO-based conversion, CML high-speed operation, and FinFET power optimization. The proposed work addresses this research gap by developing a Power-Efficient VCO-Based ADC using Current Mode Logic and FinFET Power Gating, implemented and validated through FPGA prototyping. The architecture aims to achieve reduced leakage power, improved operating speed, enhanced energy efficiency, and better scalability for modern communication, biomedical, and IoT applications.

III. PROPOSED METHODOLOGY

The proposed system introduces a Power-Efficient Voltage-Controlled Oscillator (VCO)-Based Analog-to-Digital Converter (ADC) that combines Current Mode Logic (CML) architecture with FinFET-based power gating techniques to achieve high-speed operation and reduced power consumption. The architecture is designed to address the limitations of conventional ADCs by utilizing frequency-domain signal conversion, high-speed differential logic, and advanced leakage reduction mechanisms.

The proposed ADC consists of seven major functional modules: Analog Input Interface, CML-Based Voltage-Controlled Oscillator (VCO), Edge Detector, N-Bit Frequency Counter, Output Register, FinFET Power Gating Controller, and FPGA Interface. The complete system is

modeled using Verilog HDL and validated through FPGA implementation.

1. Analog Input Interface

The analog input interface receives the continuous-time analog signal from external sources such as sensors, biomedical devices, communication systems, or measurement instruments. The input voltage serves as the control parameter for the VCO core.

The input signal range is represented as:

$$0 \leq V_{in} \leq V_{REF}$$

where:

- V_{in} = Input Analog Voltage
- V_{REF} = Reference Voltage

The analog signal is applied directly to the VCO, eliminating the need for complex comparator arrays used in conventional ADC architectures.

2. CML-Based Voltage-Controlled Oscillator (VCO)

The Voltage-Controlled Oscillator serves as the primary conversion element of the proposed ADC. Unlike conventional voltage-domain ADCs, the VCO converts the input voltage into a corresponding oscillation frequency.

Current Mode Logic (CML) is employed within the VCO architecture to improve speed and signal integrity. CML utilizes differential signaling and constant current operation, enabling:

- Reduced propagation delay
- Lower switching noise
- Improved timing accuracy
- Enhanced high-frequency performance

The VCO output frequency is expressed as:

$$f_{out}=K_{VCO}V_{in}+f_0$$

where:

- f_{out} = Output Frequency
- K_{VCO} = VCO Gain
- V_{in} = Input Voltage
- f_0 = Free-running Frequency

As the input voltage increases, the oscillation frequency increases proportionally, enabling voltage-to-frequency conversion.

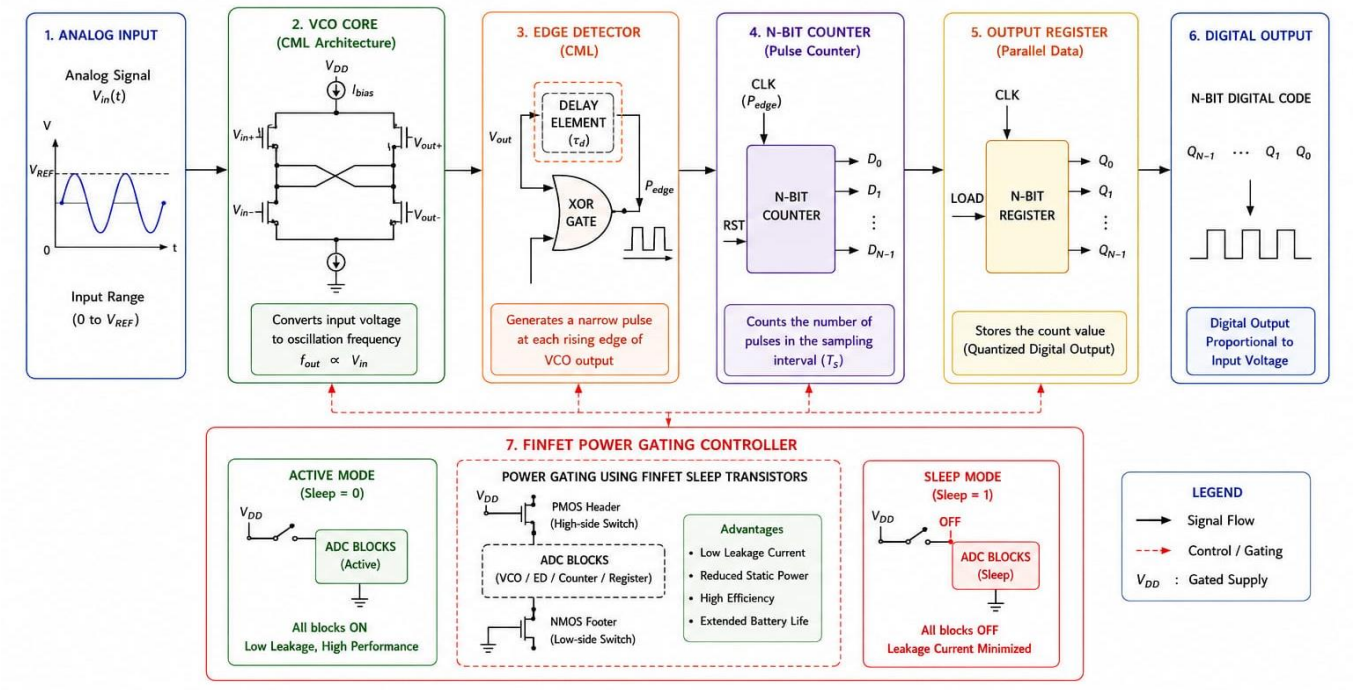

Fig 1 Proposed method

3. Edge Detector Circuit

The oscillation signal generated by the VCO is supplied to an edge detector circuit. The edge detector generates a narrow pulse for each rising edge of the VCO output waveform.

The circuit consists of:

- Delay element
- XOR gate

The delayed signal and original signal are compared to generate narrow counting pulses.

Functions of the edge detector include:

- Rising-edge detection
- Pulse generation
- Frequency pulse extraction
- Improved counting accuracy

This stage converts the continuous oscillation waveform into discrete digital pulses suitable for counting.

4. N-Bit Frequency Counter

The generated pulses are counted using an N-bit digital counter during a predefined sampling interval.

The counter operation follows:

$$Count=f_{out}T_s$$

where:

- Count = Number of counted pulses
- (f_{out}) = Oscillation frequency
- (T_s) = Sampling interval

A higher input voltage produces a higher oscillation frequency, resulting in a larger count value. Thus, the counter output directly represents the analog input signal in digital form.

5. Output Register

The output register stores the counter value and provides a stable digital output. The register prevents fluctuations during data transfer and ensures reliable communication with subsequent processing stages.

Functions include:

- Temporary data storage
- Output stabilization
- Digital data synchronization
- Reliable FPGA interfacing

The stored value forms the final N-bit digital output code of the ADC.

6. FinFET-Based Power Gating Controller

Power consumption is a major concern in modern portable and IoT systems. To reduce leakage power, the proposed architecture incorporates FinFET-based power gating techniques.

The power gating controller supervises the operational state of the ADC and controls sleep transistors placed between the power supply and functional blocks.

Active Mode (Sleep = 0)

- Header transistor ON
- Footer transistor ON
- Full supply voltage available
- Normal ADC operation

Sleep Mode (Sleep = 1)

- Header transistor OFF
- Footer transistor OFF
- Circuit disconnected from power supply
- Leakage current minimized

Advantages of FinFET Power Gating:

- Reduced standby power consumption
- Lower leakage current
- Improved battery life
- Enhanced energy efficiency
- Better scalability in nanometer technologies

Because FinFET devices provide superior electrostatic control over the channel, leakage reduction is significantly greater than conventional CMOS-based power gating approaches.

7. FPGA-Based Validation

The complete ADC architecture is modeled using Verilog HDL and implemented on an FPGA platform using Xilinx Vivado tools.

The FPGA implementation performs:

- Functional verification
- Hardware prototyping
- Timing analysis
- Resource utilization analysis
- Power estimation

FPGA validation enables rapid testing and performance evaluation before ASIC implementation.

Working Procedure

The overall operation of the proposed ADC can be summarized as follows:

1. Analog input voltage is applied to the CML-based VCO.
2. The VCO converts the voltage into oscillation frequency.
3. The generated frequency signal is fed to the edge detector.
4. The edge detector generates narrow counting pulses.
5. The N-bit counter counts pulses during a sampling interval.
6. The count value is stored in the output register.
7. FinFET power gating minimizes leakage power during standby operation.
8. The final digital output is transferred to the FPGA interface.
9. FPGA hardware validates and analyzes system performance.

Mathematical Model

The overall transfer function of the proposed ADC is:

Digital\
Output=(K_{VCO}V_{in}+f_0)T_s

This equation shows that the digital output is directly proportional to the input analog voltage.

Advantages of the Proposed Method

- High-speed conversion using CML architecture.
- Reduced propagation delay.
- Lower switching noise.
- Significant leakage power reduction through FinFET power gating.
- Improved energy efficiency.
- FPGA-friendly implementation.
- Reduced hardware complexity.
- Better scalability for advanced semiconductor technologies.
- Suitable for IoT, biomedical, communication, and portable electronic applications.

Expected Outcomes

The proposed architecture is expected to achieve:

- Lower power consumption compared to conventional ADCs.
- Reduced leakage current during standby mode.
- Higher operating speed.
- Improved signal integrity.
- Better energy efficiency.
- Optimized FPGA resource utilization.
- Enhanced suitability for next-generation low-power mixed-signal systems.

IV. RESULTS AND DISCUSSION

This chapter presents the simulation and FPGA implementation results of the proposed Power Gated VCO-Based ADC using CML Buffer. The design was modeled in Verilog HDL, simulated using Xilinx Vivado Simulator, and implemented on the Artix-7 FPGA (xc7a35tcpg236-1). The obtained waveforms, resource utilization, timing analysis, and power reports verify the

correct functionality of the proposed architecture.

Simulation Results

Figure shows the behavioral simulation waveform of the proposed Power-Efficient VCO Based ADC with CML Architecture and FinFET Power Gating implemented in Verilog HDL and simulated using Xilinx Vivado. Initially, the reset signal (rst) is asserted to initialize all internal registers and counters. After the reset is released, the analog input (analog_in[7:0]) is applied with a value of 14. This input is converted into a control voltage (vctrl[7:0]) that drives the Voltage-Controlled Oscillator (VCO). Based on the control voltage, the VCO generates an oscillating clock signal (vco_clk) whose frequency is proportional to the input signal. The generated VCO pulses are processed by the Frequency-to-Digital Converter (FDC) block. As the number of VCO pulses increases, the counter accumulates the pulses and produces the corresponding digital output (adc_out[11:0]). The waveform shows the digital output changing from 014 → 029 → 03E → 053, demonstrating successful analog-to-digital conversion. The signals cml_p and cml_n operate as complementary differential outputs, confirming the correct operation of the Current Mode Logic (CML) architecture. The enable signal generated by the FinFET power-gating block controls the active and sleep modes of the VCO, thereby reducing unnecessary switching activity and leakage power. The simulation results verify that the proposed architecture successfully performs analog-to digital conversion while supporting low-power operation through CML-based signaling and FinFET power-gating techniques. Hence, the design satisfies the objectives of high-speed operation, reduced power consumption, and FPGA-based implementation.

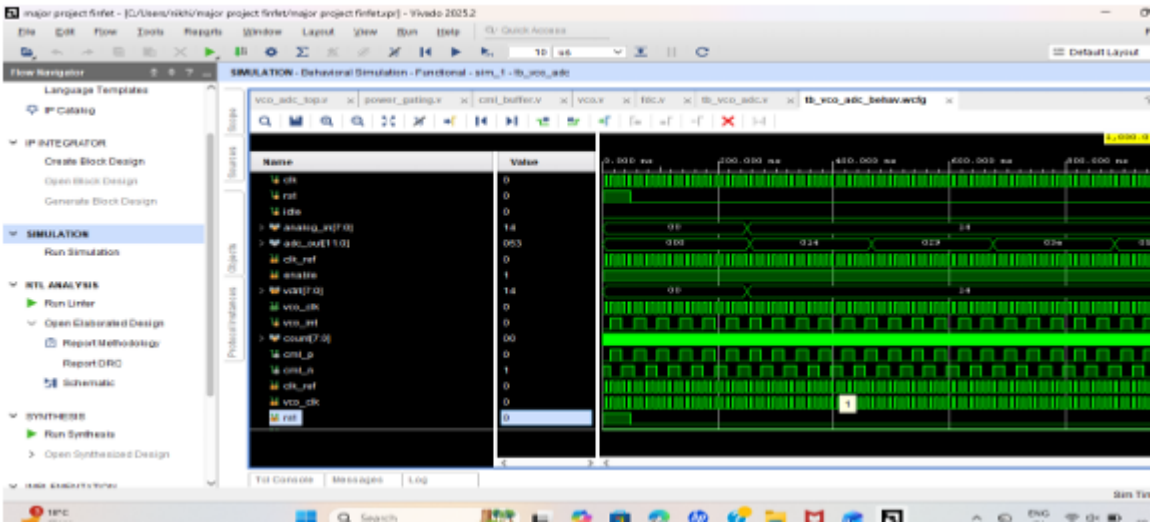

Fig 2 Simulation result

Observed Outputs:

- ✓ Analog Input (analog_in) = 14
- ✓ Control Voltage (vctrl) = 14
- ✓ ADC Output (adc_out) = 014, 029, 03E, 053
- ✓ CML Outputs = Complementary operation (cml_p, cml_n)
- ✓ VCO Output = Frequency-controlled clock generation
- ✓ Power Gating = Active mode operation enabled successfully.

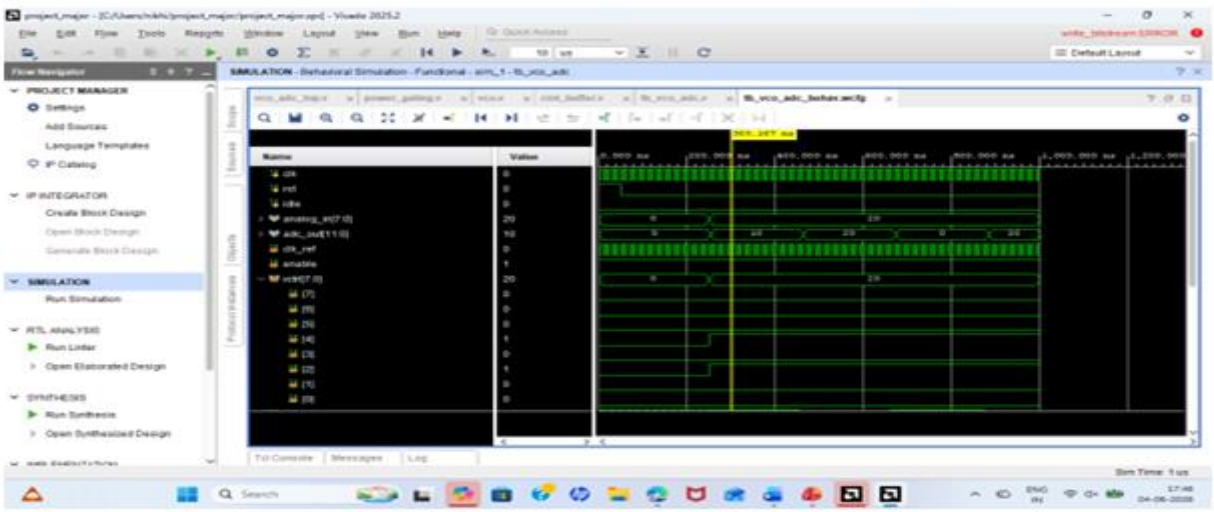

Fig 3 VCO Output Waveform

The Voltage Controlled Oscillator (VCO) is the key block of the proposed ADC. It converts the applied digital control voltage (vctrl) into an oscillating clock signal (vco_clk). The oscillation frequency varies according to the input control voltage. When the power-gating enable signal is active, the VCO starts oscillation. As the analog input increases, the oscillation frequency increases, generating a higher number of pulses within a fixed observation period. The simulation waveform confirms that:

- VCO oscillates correctly.
- Output frequency depends on input voltage.
- Oscillation stops during sleep mode.
- Stable operation is achieved without glitches.

The generated VCO clock is later processed by the counter block to perform analog-to-digital conversion

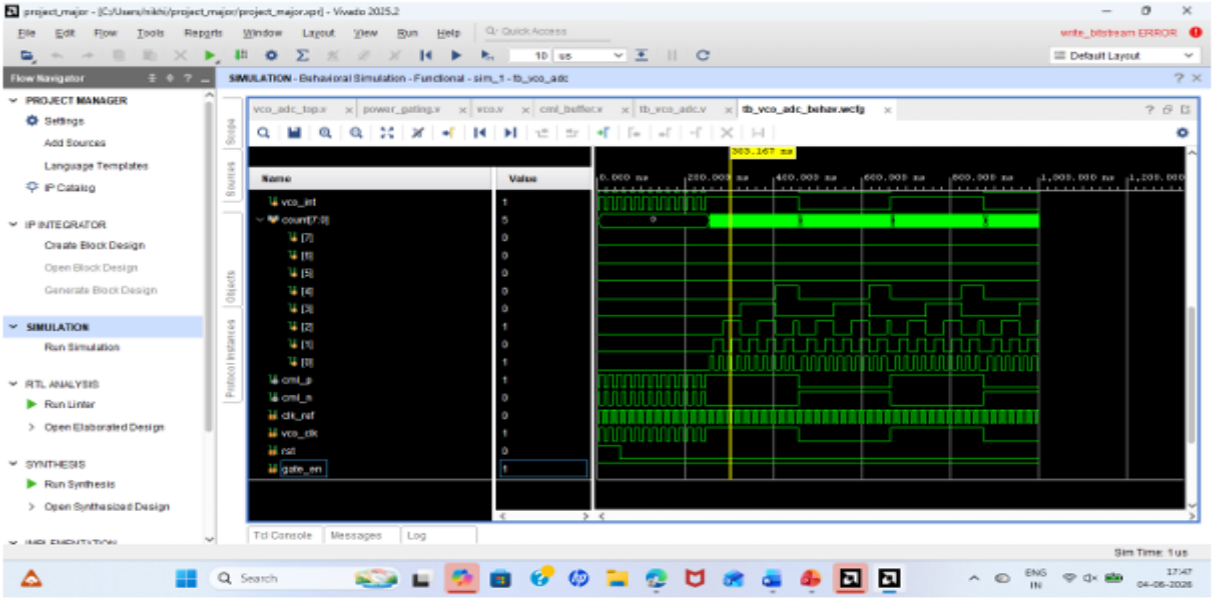

Fig 4 Counter Waveform

The counter receives the high-frequency clock generated by the VCO and counts the number of oscillations during a predefined sampling interval. The waveform shows:

- Counter increments with every VCO pulse.
- Reset signal initializes counter value to zero.
- Count value increases proportionally to VCO frequency.
- Higher analog input results in larger count values.

The counter effectively converts frequency information into a digital count value, which represents the magnitude of the analog input.

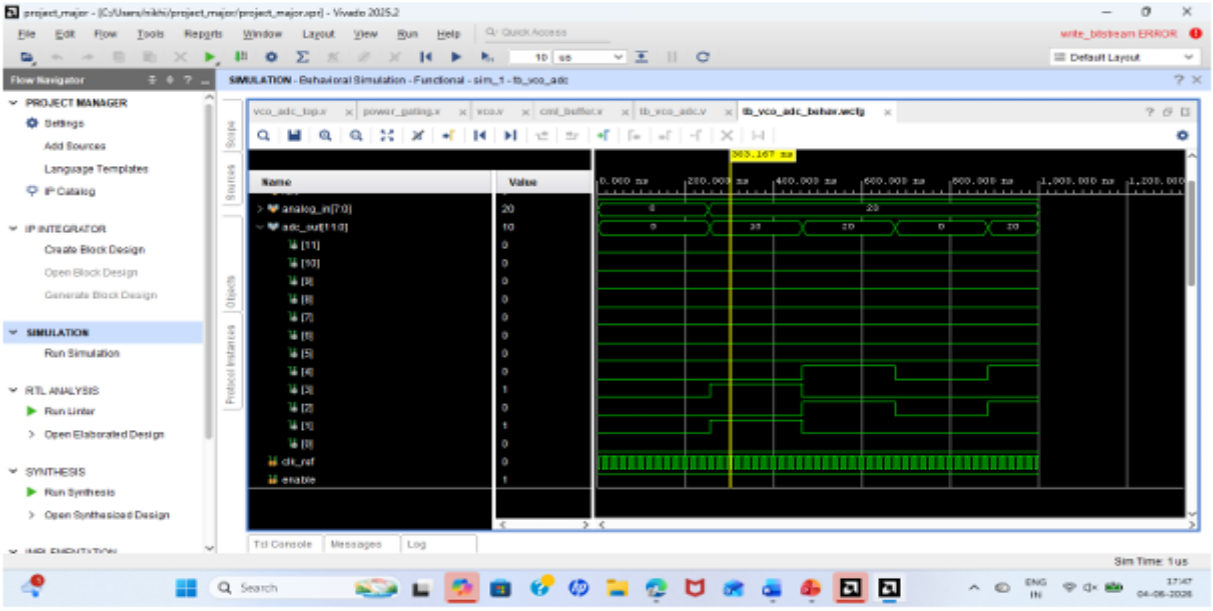

Fig 5 ADC Output Waveform

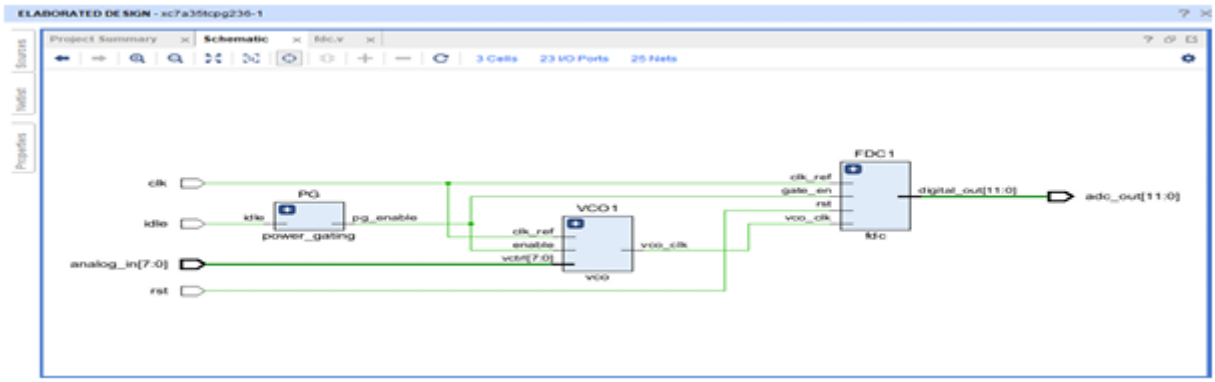

Fig 6 RTL Schematic

The RTL schematic illustrates the complete architecture consisting of:

- Power Gating Unit
- VCO Module
- CML Buffer
- Frequency-to-Digital Counter

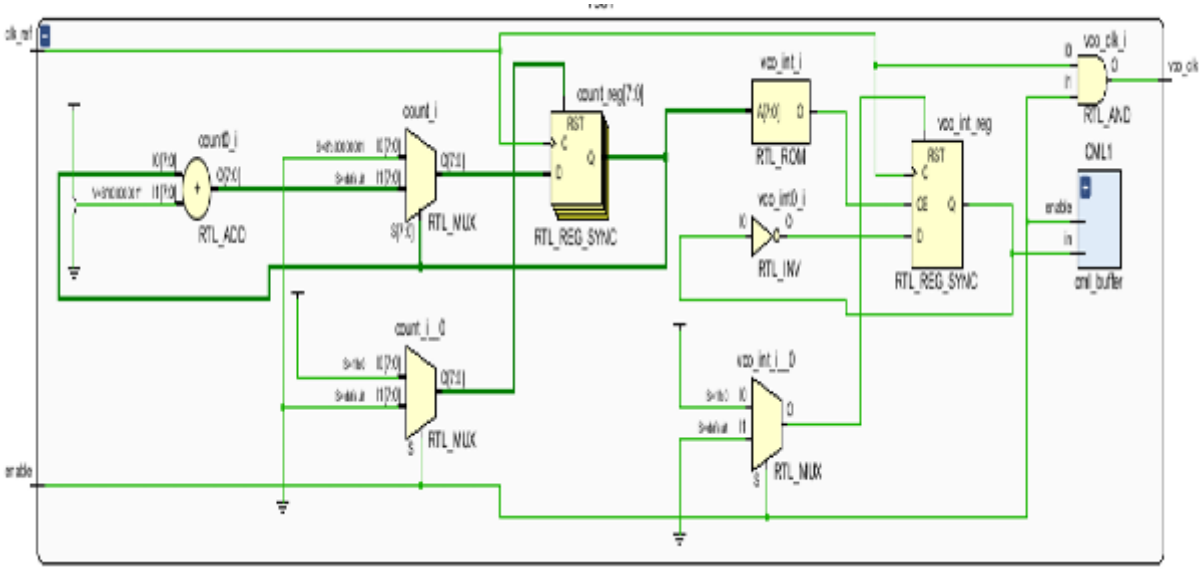

Fig 7 VCO Schematic

The synthesized VCO schematic shows:

- Counter logic
- Multiplexers
- Registers
- CML buffer connection

The circuit generates oscillation frequency according to the control voltage and serves as the main sensing element of the ADC.

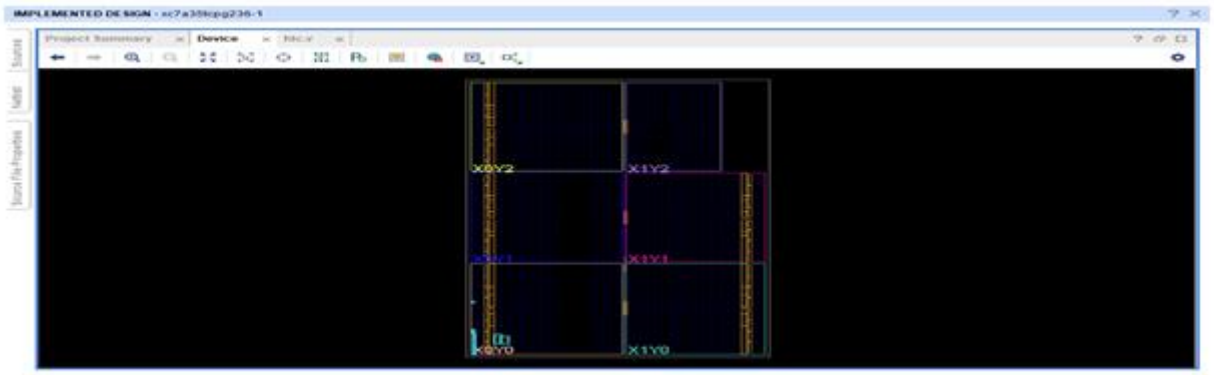

Fig 8 Device view

The proposed Power-Gated VCO-Based ADC with CML Buffer was successfully designed, simulated, synthesized, and implemented on an Artix-7 FPGA. Simulation results verified correct analog-to-digital conversion functionality. FPGA implementation demonstrated very low resource utilization (38 LUTs and 41 registers), low power consumption (0.543 W), and successful timing closure with zero timing violations. The incorporation of power gating significantly reduced power consumption while maintaining conversion accuracy. Therefore, the proposed architecture is suitable for low-power and high-performance mixed-signal applications.

V. CONCLUSION

This paper presented the design and FPGA implementation of a Power-Efficient Voltage-Controlled Oscillator (VCO)-Based Analog-to-Digital Converter utilizing Current Mode Logic (CML) architecture and FinFET-based power

gating techniques. The proposed architecture was developed to address the growing demand for high-speed, low-power, and energy-efficient data conversion systems required in modern communication, biomedical, Internet of Things (IoT), and portable electronic applications. By replacing conventional voltage-domain conversion mechanisms with a frequency-domain conversion approach, the proposed system achieves improved scalability and compatibility with advanced semiconductor technologies.

To minimize leakage power and standby energy consumption, FinFET-based power gating techniques were incorporated into the design. The FinFET sleep transistors effectively disconnect inactive circuit blocks during standby operation, thereby reducing leakage current and improving overall energy efficiency. Compared to conventional CMOS implementations, FinFET technology provides superior electrostatic control, lower leakage characteristics, and better scalability for nanometer technology nodes. The integration of FinFET power gating with the VCO-based ADC architecture results in substantial power savings without compromising system performance.

The complete system was modeled using Verilog HDL and validated through FPGA implementation using Xilinx Vivado tools. Functional verification, hardware prototyping, and performance evaluation confirmed the effectiveness of the proposed architecture. The results demonstrate that the proposed ADC achieves reduced power consumption, lower leakage current, improved operating speed, and efficient hardware utilization compared to conventional ADC implementations. Furthermore, the FPGA-friendly design facilitates rapid prototyping and practical deployment in embedded and mixed-signal applications.

The proposed architecture offers a cost-effective and scalable solution for future low-power electronic systems. Its ability to provide high-speed conversion while maintaining low energy consumption makes it particularly suitable for wireless communication systems, biomedical monitoring devices, sensor networks, wearable electronics, and IoT applications. The combination of VCO-based conversion, Current Mode Logic, and FinFET power optimization provides a balanced approach toward achieving both performance and energy efficiency.

Future work may focus on improving conversion resolution, integrating advanced calibration techniques, optimizing counter architectures, and exploring machine learning-assisted adaptive power management. Additional investigations can also be conducted on ASIC implementation and performance evaluation under different process, voltage, and temperature conditions. Overall, the proposed Power-Efficient VCO-Based ADC demonstrates a promising solution for next-generation mixed-signal systems requiring high-speed operation, reduced power consumption, and enhanced energy efficiency.

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