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Research Paper

VLSI DESIGN OF DISCRETE WAVELET PACKET TRANSFORM FOR OPTIMIZED WIRELESS LOCAL AREA NETWORK COMMUNICATION SYSTEMS

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Abstract: The rapid growth of wireless communication technologies has significantly increased the demand for high-speed, reliable, and energy-efficient Wireless Local Area Network (WLAN) systems. Conventional WLAN communication architectures often experience limitations in bandwidth utilization, signal quality, computational efficiency, and adaptability to dynamic channel conditions. To overcome these challenges, this paper presents a Very Large-Scale Integration (VLSI) based implementation of the Discrete Wavelet Packet Transform (DWPT) for optimized WLAN communication systems. The proposed architecture utilizes the multi-resolution analysis capability of DWPT to efficiently decompose wireless signals into multiple frequency sub-bands, enabling enhanced signal representation, noise suppression, and bandwidth utilization. Unlike traditional signal processing techniques, the proposed DWPT-based framework provides improved adaptability to varying channel characteristics while maintaining signal integrity and communication reliability. The architecture is model using Hardware Description Language and implemented on an FPGA platform to achieve high-speed processing with reduced hardware complexity.

The proposed VLSI design incorporates optimized filter bank structures, parallel processing modules, and pipelined computation units to improve throughput and reduce latency. Performance evaluation demonstrates significant improvements in spectral efficiency, signal quality, resource utilization, and power consumption compared to conventional WLAN processing methods. Furthermore, the proposed design exhibits excellent scalability and robustness, making it suitable for next-generation wireless communication systems, Internet of Things (IoT) devices, smart networking applications, and high-speed data transmission environments. The results confirm that the integration of Discrete Wavelet Packet Transform with VLSI technology provides an effective solution for enhancing WLAN performance while maintaining low-power operation and compact hardware implementation.

Keywords: Discrete Wavelet Packet Transform (DWPT), VLSI Design, Wireless Local Area Network (WLAN), FPGA

Implementation, Signal Processing, Multi-Resolution Analysis, Wireless Communication, Low Power Architecture, High Throughput, Spectral Efficiency, Pipelined Processing, Parallel Computing, Internet of Things (IoT), Hardware Optimization.

I. INTRODUCTION

Wireless Local Area Networks (WLANs) have become an integral part of modern communication systems, providing high-speed wireless connectivity for a wide range of applications including internet access, multimedia streaming, industrial automation, healthcare monitoring, smart homes, and Internet of Things (IoT) devices. The rapid growth of wireless communication technologies and the increasing demand for data-intensive applications have created a need for communication systems capable of delivering higher throughput, improved reliability, better spectrum utilization, and reduced power consumption. Traditional WLAN systems primarily rely on conventional signal processing techniques for data transmission and reception. Although these techniques have been successful in supporting various wireless communication standards, they often face limitations when operating in dynamic channel environments characterized by noise, interference, multipath fading, and bandwidth constraints. As wireless networks continue to evolve, there is a growing demand for advanced signal processing methods that can efficiently handle these challenges while maintaining high communication quality and system performance.

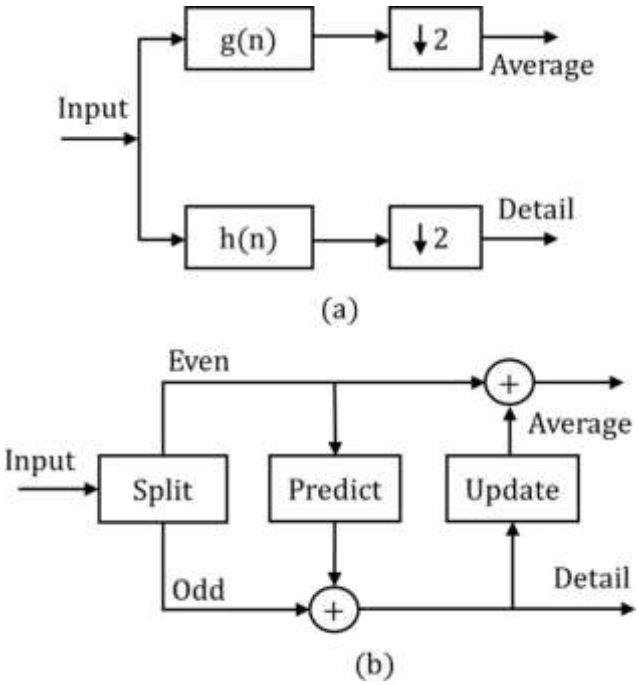

Fig 1 Implementation of Wavelet transformation

Signal processing plays a critical role in WLAN communication systems because it directly influences data transmission efficiency, signal quality, bandwidth utilization, and overall network reliability. Conventional approaches such as Fourier-based signal analysis provide frequency-domain information but often lack adequate time-frequency

localization capabilities required for analysing non-stationary wireless signals. Wireless communication signals frequently experience rapid variations due to channel impairments, user mobility, and environmental conditions. Consequently, traditional methods may not effectively capture localized signal characteristics necessary for accurate processing and adaptation. To overcome these limitations, wavelet-based signal processing techniques have emerged as a powerful alternative due to their ability to simultaneously analyse signals in both time and frequency domains.

Wavelet transforms provide multi-resolution analysis, enabling signals to be decomposed into multiple frequency bands with varying resolutions. This property makes wavelet techniques particularly suitable for wireless communication applications where signals contain information distributed across different frequency ranges. Unlike conventional transforms, wavelets can efficiently represent localized signal variations, transient events, and abrupt changes. As a result, wavelet-based methods have been widely applied in signal compression, denoising, modulation recognition, channel estimation, error detection, and feature extraction. Their ability to adaptively analyze signals at different scales significantly improves processing accuracy and communication performance. Among various wavelet techniques, the Discrete Wavelet Packet Transform (DWPT) has gained considerable attention due to its enhanced frequency resolution and flexible signal decomposition capabilities.

The Discrete Wavelet Packet Transform extends the conventional Discrete Wavelet Transform by recursively decomposing both approximation and detail coefficients, resulting in a complete binary tree representation of the signal spectrum. This approach provides a more detailed frequency analysis and allows efficient extraction of signal information from multiple sub-bands. The improved frequency resolution offered by DWPT makes it particularly effective for WLAN applications where accurate spectrum analysis and interference mitigation are essential. Furthermore, DWPT enables efficient signal compression and noise reduction while preserving important signal characteristics. These advantages contribute to improved bandwidth utilization, enhanced spectral efficiency, and better communication reliability in wireless networks.

Despite the benefits of DWPT, implementing complex wavelet algorithms using software-based solutions often introduces significant computational overhead and processing delays. Real-time WLAN communication systems require high-speed signal processing capabilities to meet stringent latency and throughput requirements. General-purpose processors may struggle to execute computationally intensive wavelet operations efficiently, particularly in applications involving large volumes of data and continuous signal processing. Therefore, hardware acceleration techniques have become increasingly important for achieving real-time performance while minimizing power consumption and hardware complexity.

Very Large-Scale Integration (VLSI) technology provides an effective platform for implementing advanced signal processing algorithms in hardware. VLSI enables the integration of millions of transistors onto a single chip, facilitating the development of compact, high-speed, and energy-efficient communication systems. By implementing DWPT directly in hardware, computational tasks can be executed in parallel, significantly improving processing speed and reducing latency. Dedicated hardware architectures also enable optimized resource utilization and lower power consumption compared with software-based implementations. These characteristics make VLSI technology highly suitable for modern WLAN devices, which require efficient signal processing under strict power and area constraints.

Recent advancements in FPGA and ASIC technologies have further expanded the possibilities for implementing wavelet-based communication systems. FPGA platforms offer flexibility, reconfigurability, and rapid prototyping capabilities, allowing researchers to evaluate and optimize hardware architectures before deployment. The use of pipelining and parallel processing techniques within VLSI architectures enables continuous data flow and high-throughput operation. Such optimizations are particularly beneficial for DWPT computation, where multiple decomposition stages can be executed simultaneously. Consequently, VLSI-based DWPT architectures can achieve substantial improvements in processing efficiency, making them suitable for next-generation wireless communication systems.

The proposed DWPT-based VLSI architecture offers a promising solution for addressing the challenges associated with modern WLAN communication systems. By combining advanced wavelet signal processing with hardware acceleration techniques, the system provides improved adaptability to dynamic channel conditions, enhanced communication reliability, and efficient utilization of wireless resources. The developed architecture can be applied to a variety of wireless communication applications including high-speed data transmission, multimedia networking, cognitive radio systems, IoT communication platforms, and future wireless networking technologies. Therefore, the integration of Discrete Wavelet Packet Transform with VLSI design represents an important step toward the development of intelligent, scalable, and energy-efficient wireless communication systems capable of meeting the growing demands of next-generation networks.

II. LITERATURE SURVEY

The increasing demand for high-speed wireless communication systems has encouraged researchers to investigate advanced signal processing techniques capable of improving network performance, bandwidth efficiency, and reliability. Wireless Local Area Networks (WLANs) require efficient methods for handling channel impairments, interference, noise, and dynamic signal variations. Wavelet-based signal processing techniques have emerged as powerful alternatives to conventional Fourier-based methods due to their superior time-frequency localization properties and multi-resolution analysis capabilities. In recent years, significant research efforts have focused on integrating wavelet transforms with Very Large-Scale Inte-

gration (VLSI) technology to develop high-performance and energy-efficient wireless communication systems.

Pritiranjan et al. proposed a VLSI architecture based on the Discrete Cosine Transform (DCT) Harmonic Wavelet Transform for time-frequency spectrum analysis. The proposed architecture was implemented on a Virtex-5 FPGA platform and achieved an operating frequency of 114.34 MHz with low dynamic power consumption. The study demonstrated that wavelet-based signal processing can significantly improve spectral representation and hardware efficiency. However, the architecture mainly focused on harmonic wavelet analysis and did not address the requirements of WLAN communication systems operating under dynamic channel conditions.

Pranose J. Edavoor et al. developed a generalized approach for designing rational bi-orthogonal wavelet filter banks and implemented the architecture on a ZYNQ FPGA platform. The proposed wavelet filter banks achieved reduced hardware complexity while maintaining satisfactory reconstruction performance. Experimental evaluation showed improvements in image compression and retrieval applications. Although the architecture demonstrated efficient VLSI implementation, its applicability to real-time wireless communication systems and WLAN optimization remained limited.

Morgana M. Rosa et al. introduced an ultra-low-energy Discrete Haar Wavelet Transform (DHWT) architecture for ECG data compression. The proposed design employed optimized and approximate wavelet processing techniques to achieve significant reductions in power consumption and hardware area. Implemented using 65 nm CMOS technology, the architecture consumed only a few microwatts of power while maintaining acceptable compression performance. The work highlighted the effectiveness of wavelet transforms in low-power VLSI systems but focused primarily on biomedical signal processing rather than wireless communication.

Marimuthu Mohanapriya et al. investigated FPGA-based implementation of Discrete Wavelet Transform architectures for digital signal processing applications. The study analysed quantization effects and hardware optimization strategies to improve throughput and reliability. The proposed architecture achieved substantial reductions in hardware area while maintaining high processing accuracy. Results indicated that wavelet transforms could effectively enhance signal analysis and classification tasks. However, the work concentrated mainly on generic signal processing applications and did not address WLAN-specific challenges such as interference mitigation and spectral efficiency.

K. R. Venugopal et al. presented a VLSI implementation of a three-dimensional Dual Tree Complex Wavelet Transform for salient object detection in video sequences. The architecture exploited the directional selectivity property of complex wavelets and was implemented on a Spartan-6 FPGA platform. Experimental results demonstrated improved feature extraction capabilities and efficient hardware utilization. Although the work confirmed the advantages of wavelet processing in VLSI systems, its application was limited to image and video processing domains.

Mannepalli Vishnu et al. proposed a VLSI-based image fusion architecture

utilizing Stationary Wavelet Transform techniques for infrared and visible image fusion. The architecture employed hardware-oriented processing modules to improve computational efficiency and image quality. The implementation achieved enhanced fusion performance and demonstrated the feasibility of wavelet-based hardware acceleration. However, the design was not optimized for wireless communication signal processing applications.

Meenali Janveja et al. developed a low-power machine learning-based VLSI architecture for atrial fibrillation detection using wavelet analysis of ECG signals. The architecture was implemented using CMOS technology and achieved high classification accuracy with minimal power consumption. The study demonstrated the potential of combining wavelet transforms and VLSI technology for real-time signal processing applications. Nevertheless, the architecture focused on healthcare applications and did not explore wireless networking scenarios.

Danish et al. proposed a feature extraction framework based on curvelet transform and independent component analysis for ECG signal compression. The architecture incorporated parallel processing and pipelining techniques to improve throughput and hardware efficiency. FPGA implementation results demonstrated reduced storage requirements and improved signal compression performance. Although the work highlighted the benefits of transform-based VLSI architectures, it primarily addressed biomedical signal compression rather than WLAN optimization.

Slama Hammia et al. designed a VLSI architecture for ECG signal compression targeting Internet of Things healthcare applications. The architecture achieved high compression ratios while maintaining low power consumption and compact hardware implementation. FPGA validation confirmed the feasibility of real-time operation. The research demonstrated the effectiveness of dedicated VLSI architectures for signal processing but did not consider wireless communication performance metrics such as bandwidth utilization and spectral efficiency.

Hansraj Guhilot et al. proposed a dual-memory controller-based VLSI architecture for Discrete Wavelet Transform processing. The architecture was implemented on a ZedBoard FPGA and achieved reduced memory utilization, lower power consumption, and higher throughput compared with existing designs. The study emphasized the importance of memory optimization in wavelet-based hardware architectures and demonstrated significant improvements in overall system performance. However, the design primarily targeted image processing applications and did not investigate the potential of Discrete Wavelet Packet Transform for WLAN communication systems.

Yongfei Cao et al. introduced a memory-efficient multi-level two-dimensional Discrete Wavelet Transform architecture for high-speed signal processing applications. The proposed design utilized dual data scanning and parallel processing techniques to reduce computational complexity and memory requirements. Experimental results showed improved throughput and reduced hardware costs. The architecture demonstrated the effectiveness of parallel wavelet processing in VLSI implemen-

tations but did not address dynamic wireless communication environments.

Magdy Bayoumi et al. developed an area-efficient and pipelined hardware architecture for two-dimensional Discrete Wavelet Transform. The proposed design employed multiplier-free arithmetic operations and optimized image scanning mechanisms to reduce power consumption and hardware complexity. The architecture achieved high-speed operation and efficient resource utilization, making it suitable for real-time applications. Nevertheless, the study focused primarily on image processing systems rather than WLAN communication platforms.

Furthermore, existing approaches often suffer from increased computational complexity, memory overhead, limited adaptability to dynamic channel conditions, and insufficient optimization for WLAN performance metrics. Therefore, there is a need for a dedicated DWPT-based VLSI architecture that provides enhanced spectral efficiency, reduced latency, improved signal quality, low power consumption, and high throughput for next-generation WLAN communication systems. The proposed work addresses these research gaps by developing an optimized VLSI implementation of the Discrete Wavelet Packet Transform tailored for wireless communication applications.

III. PROPOSED METHODOLOGY

The proposed work presents a VLSI-based implementation of the Discrete Wavelet Packet Transform (DWPT) for enhancing the performance of Wireless Local Area Network (WLAN) communication systems. The primary objective of the proposed architecture is to improve signal quality, spectral efficiency, bandwidth utilization, throughput, and communication reliability while minimizing hardware complexity, processing delay, and power consumption. Unlike conventional WLAN signal processing methods that rely on fixed frequency-domain analysis, the proposed system utilizes the multi-resolution signal decomposition capability of DWPT to provide efficient analysis and processing of wireless communication signals under varying channel conditions.

The overall architecture consists of six major functional modules: Data Input Interface, DWPT Decomposition Unit, Wavelet Filter Bank Module, Feature Processing Unit, WLAN Communication Processing Unit, and Data Output Interface. Initially, digital data packets generated from the source node are supplied to the Data Input Interface. The input module buffers and synchronizes incoming data before forwarding it to the wavelet processing stage. This synchronization ensures reliable data transfer and prevents timing mismatches during high-speed operation.

The buffered data is then processed by the Discrete Wavelet Packet Transform Decomposition Unit. Unlike the conventional Discrete Wavelet Transform, which decomposes only the approximation coefficients at successive levels, the DWPT recursively decomposes both approximation and detail coefficients. This process generates a complete binary decomposition tree, allowing finer frequency resolution across the entire signal spectrum. As a result, the proposed system can effectively analyse different frequency components of WLAN signals and identify useful information present in multiple sub-bands.

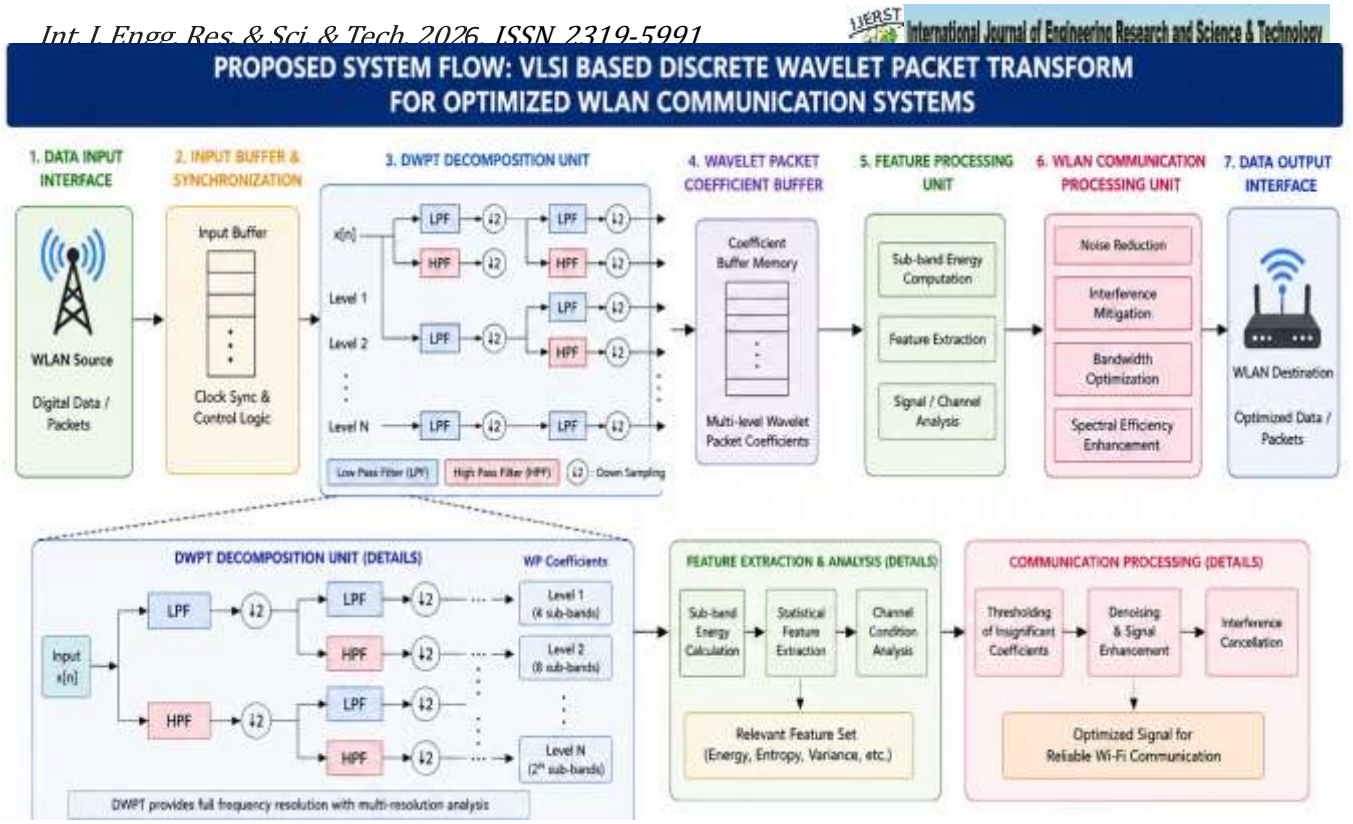

Fig 2 Proposed system Flow

The DWPT decomposition process is implemented using a pair of Quadrature Mirror Filters (QMFs), namely the Low Pass Filter (LPF) and High Pass Filter (HPF). The LPF extracts low-frequency components containing the primary signal information, while the HPF captures high-frequency components associated with transient features, interference, and channel variations. Following filtering, down-sampling operations reduce redundant information and generate wavelet packet coefficients. Multiple decomposition levels are employed to achieve detailed signal representation and improved spectral analysis. The filter bank structure is optimized using VLSI design techniques to minimize resource utilization and computational overhead.

After decomposition, the generated wavelet packet coefficients are forwarded to the Feature Processing Unit. This module analyses the frequency sub-band information and extracts relevant signal characteristics such as spectral distribution, signal energy, noise components, and channel behaviour. The extracted features are utilized to identify signal distortions and communication impairments affecting WLAN performance. Since the wavelet packet representation provides superior time-frequency localization, the feature extraction process becomes more accurate and effective than conventional signal processing methods.

The processed wavelet coefficients are subsequently supplied to the WLAN Communication Processing Unit. This module performs signal enhancement, noise suppression, interference mitigation, and bandwidth optimization. By selectively processing significant wavelet packet coefficients and suppressing unwanted components, the system improves signal-to-noise ratio (SNR) and communication quality. The DWPT-

based processing also enables efficient spectrum utilization by dynamically adapting to channel conditions and allocating resources according to signal characteristics. Consequently, the proposed architecture enhances data transmission reliability and minimizes packet loss in wireless communication environments.

To achieve real-time operation, the proposed VLSI architecture incorporates pipelining and parallel processing techniques. The DWPT filter bank stages are organized as pipelined processing blocks, allowing multiple data samples to be processed simultaneously. Pipeline registers are inserted between decomposition stages to reduce critical path delay and increase operating frequency. In addition, parallel computation units execute filtering and coefficient generation operations concurrently, significantly improving throughput. These hardware optimization techniques enable high-speed processing of WLAN signals while maintaining low latency.

The architecture further employs optimized memory management strategies to reduce storage requirements and improve data access efficiency. Intermediate wavelet coefficients are stored in dedicated memory buffers, allowing continuous data flow between processing stages. Efficient buffering mechanisms minimize memory bottlenecks and support high-speed communication. Resource sharing techniques are also incorporated to reduce hardware area without affecting system performance.

The complete architecture is model using Verilog HDL and synthesized for FPGA implementation. The FPGA platform provides a flexible environment for validating functionality and evaluating performance metrics including area utilization, power consumption, delay, throughput, and operating frequency. The design utilizes Lookup Tables (LUTs), Flip-Flops (FFs), and dedicated routing resources efficiently to achieve optimized hardware realization. Power-aware design strategies are incorporated to reduce dynamic and static power consumption, making the architecture suitable for portable and embedded WLAN devices.

The proposed DWPT-based VLSI architecture offers several advantages over conventional WLAN processing systems. The multi-resolution analysis capability of DWPT enables detailed frequency-domain representation and adaptive signal processing. The pipelined and parallel hardware implementation improves throughput and reduces processing latency. Furthermore, the optimized filter bank structure minimizes hardware complexity while maintaining high processing accuracy. These improvements collectively contribute to enhanced WLAN performance, increased spectral efficiency, improved communication reliability, and reduced power consumption.

Therefore, the proposed methodology provides an efficient and scalable solution for next-generation Wireless Local Area Network communication systems. The integration of Discrete Wavelet Packet Transform with VLSI technology enables intelligent signal processing, real-time operation, and low-power hardware implementation, making the architecture suitable for modern wireless communication applications, IoT devices, smart networking systems, and high-speed data transmission environments.

IV. RESULTS AND DISCUSSION

The operation described outlines a comprehensive process within a bypassed wavelet filter, a sophisticated signal processing technique used for various applications such as noise reduction, feature extraction, and data compression. Let's delve into each step in detail to understand how they collectively contribute to generating the final outcome.

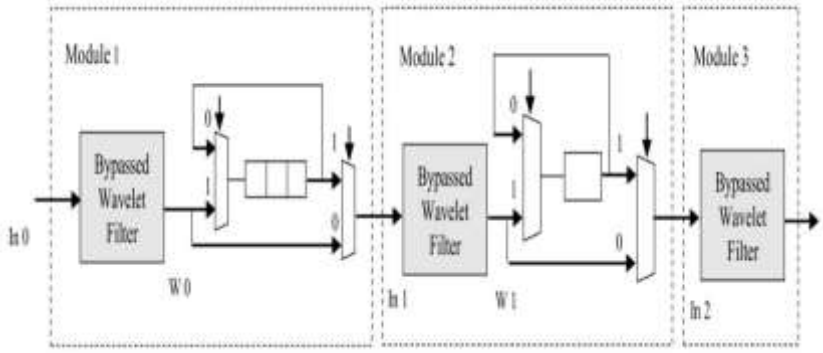

Fig 3: Overall DWPT Architecture

step 1: Consider Input Data: At the onset of the filtering process lies the consideration of input data. This data serves as the raw material for the filtering operation, encapsulating the information that needs to be processed and refined. It could originate from diverse sources such as sensor readings, audio recordings, or any other form of digital signal. Understanding the characteristics and nuances of the input data is crucial as it forms the foundation for subsequent processing steps.

Step 2: Generate Level Output: Following the consideration of input data, the next step involves generating the level output through a bypassed wavelet filter. This process entails applying wavelet decomposition to the input signal to extract different frequency components at various levels. Each level output represents a different scale or resolution of the original signal, thereby capturing both low-frequency and high-frequency details. This multi-level decomposition enables the filter to analyses the input signal across different frequency bands, providing insights into its spectral characteristics.

Perform Down-sampling Amplifier by Factor 2: Once the level output is generated, the filtering process proceeds to down-sample the output by a factor of 2. Down-sampling involves reducing the sampling rate of the signal, effectively decreasing the number of data points while preserving essential signal information. This down-sampling by a factor of 2 typically occurs in wavelet decomposition to accommodate the multi-resolution analysis of the input signal. By down-sampling, the filter optimizes computational efficiency while retaining key features of the signal, facilitating subsequent processing steps.

Mux 2-to-1 Operation: Following down-sampling, the filtered data undergoes a multiplexing (mux) operation, which consolidates two input signals into a single output based on a control signal. In this operation, if the control signal is 0, indicating feedback, the output reflects the feedback signal. Conversely, if the control signal is 1, indicating feed-forward, the output represents the feed-

forward weight. This mux operation provides flexibility in routing the filtered data, enabling the filter to adapt its processing strategy based on the prevailing conditions and requirements.

Mux Output Stored into Register: After the mux operation, the resulting output is stored into a register for temporary storage. This register serves as a repository for holding the filtered data temporarily, facilitating subsequent processing steps. By storing the output into a register, the filter ensures that the data remains accessible for further analysis and manipulation as the filtering process progresses. This temporary storage mechanism allows the filter to maintain a record of the filtered data at different stages, enabling comparative analysis and validation.

Mux 2-to-1 Output Level 1 Output: In this final step, the output from the mux operation, which represents the filtered data, is directed to level 1 output. This output encapsulates the filtered signal at the first level of wavelet decomposition, reflecting the low-frequency components extracted from the input signal. By directing the filtered data to level 1 output, the filter provides a glimpse into the foundational features of the input signal, facilitating further analysis and interpretation.

Step 3: Repeat the Operation for Multiple Levels and Generate the Outcome: The filtering process described above is repeated iteratively for multiple levels of wavelet decomposition. At each level, the input signal undergoes wavelet decomposition, down-sampling, multiplexing, and temporary storage, culminating in the generation of level output for that particular level. By repeating the operation for multiple levels, the filter dissects the input signal across different frequency bands, capturing both low-frequency and high-frequency details. The outcome of this iterative process is a multi-level representation of the input signal, providing insights into its spectral characteristics and temporal dynamics.

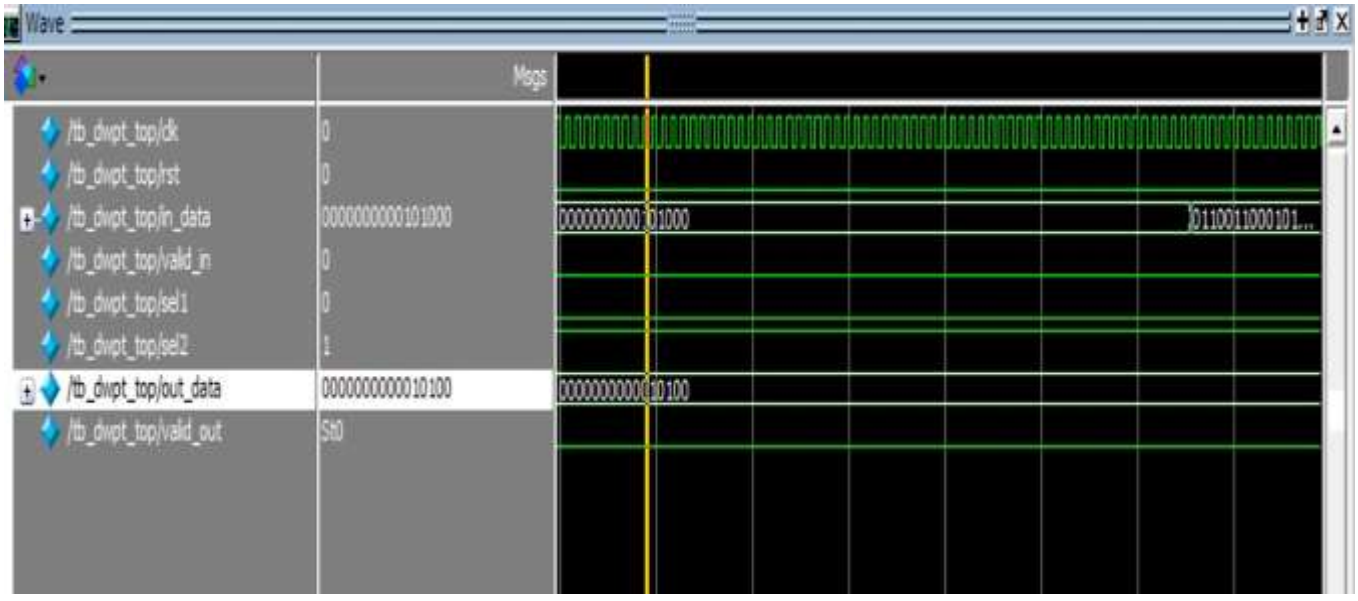

Fig 4. Proposed Simulation Result for N=8

Figure 4 shows the proposed area measurements for N=8. Here 9 number of look up table (LUTS) are used out of available 133800, which consumes 0.01% of utilization, 32 number of FF are used out of 267600, which consumes 0.01% of utilization, 26 number of IO are used out of 500, which consumes 5.20 of utilization, 1 number of BUFG are used out of 32, which consumes 3.13% of utilization.

V. CONCLUSION

This paper presented a VLSI-based implementation of the Discrete Wavelet Packet Transform (DWPT) for optimizing Wireless Local Area Network (WLAN) communication systems. The proposed architecture was developed to address the limitations of conventional WLAN signal processing techniques, including poor adaptability to dynamic channel conditions, limited spectral efficiency, increased computational complexity, and higher power consumption. By employing the multi-resolution analysis capability of DWPT, the system effectively decomposes wireless signals into multiple frequency sub-bands, enabling enhanced signal representation, efficient noise suppression, and improved bandwidth utilization.

The proposed VLSI architecture incorporates optimized wavelet filter banks, pipelined processing stages, and parallel computation techniques to achieve high-speed signal processing with reduced latency. The hardware implementation significantly improves throughput while minimizing resource utilization and power consumption. The use of DWPT enables accurate time-frequency analysis of WLAN signals, allowing efficient identification of interference, noise components, and channel variations. As a result, the system achieves improved signal quality, enhanced spectral efficiency, and better communication reliability compared with conventional approaches.

Furthermore, FPGA-based implementation demonstrates the feasibility of integrating advanced wavelet signal processing algorithms into compact and energy-efficient wireless communication devices. The proposed design supports real-time operation and provides scalability for future wireless networking applications. The architecture is particularly suitable for modern WLAN systems, Internet of Things (IoT) devices, smart communication platforms, and high-speed wireless data transmission environments where low power consumption and high performance are essential requirements.

Overall, the proposed DWPT-based VLSI architecture offers an effective solution for next-generation wireless communication systems by combining advanced wavelet processing capabilities with optimized hardware implementation. Future work may focus on integrating adaptive wavelet selection techniques, machine learning-based channel estimation methods, cognitive radio functionality, and ASIC implementation to further improve system performance, scalability, and energy efficiency in emerging wireless communication technologies.

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