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Research Paper

A NOVEL DOUBLE-TAIL DYNAMIC COMPARATOR FOR LOW-POWER HIGH-SPEED ADCS

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Abstract: Analog-to-Digital Converters (ADCs) are essential components in modern communication, signal processing, biomedical, and embedded systems. The performance of an ADC largely depends on the efficiency of its comparator, which acts as the decision-making element during signal conversion. Conventional dynamic comparators provide high speed and low static power consumption but suffer from increased delay, limited operation at low supply voltages, and higher power dissipation. This paper presents the design and analysis of a low-power high-speed dynamic comparator based on a modified double-tail architecture. The proposed comparator enhances regenerative feedback by incorporating additional cross-coupled control transistors, thereby significantly reducing latch regeneration time and improving comparison speed. The architecture operates efficiently under low-voltage conditions while maintaining low power consumption and high accuracy. Detailed analysis of comparator delay, power consumption, and operating characteristics is carried out using VLSI design methodologies. Simulation results demonstrate that the proposed design achieves faster decision-making, reduced propagation delay, lower power dissipation, and improved overall performance compared to conventional dynamic comparators. The proposed comparator is suitable for high-speed and low-power ADC applications used in portable electronics, wireless communication systems, biomedical instruments, and Internet of Things (IoT) devices.

Keywords: Dynamic Comparator, Analog-to-Digital Converter (ADC), Double-Tail Comparator, Low-Power VLSI Design, High-Speed Comparator, CMOS Technology, FPGA Implementation, Regenerative Latch, Delay Reduction, Mixed-Signal Circuits.

I. INTRODUCTION

The rapid advancement of modern electronic systems has significantly increased the demand for high-speed, low-power, and area-efficient integrated circuits. Analog-to-Digital Converters (ADCs) play a crucial role in bridging the gap between the analog real world and digital processing systems. ADCs are extensively used in wireless communication systems, biomedical instrumentation, image processing, radar

systems, sensor networks, consumer electronics, and Internet of Things (IoT) applications. The overall performance of an ADC largely depends on the speed, accuracy, and power consumption of its comparator, which acts as the decision-making element during the conversion process.

A comparator is one of the most fundamental building blocks in mixed-signal integrated circuits. It compares two input voltages and produces a digital output indicating which input is larger. High-speed ADC architectures such as Flash ADCs, Pipeline ADCs, and Successive Approximation Register (SAR) ADCs require comparators capable of operating at high frequencies while consuming minimal power. As semiconductor technologies continue to scale down into deep submicron regions, supply voltages are reduced to minimize power consumption. However, reduced supply voltages create significant challenges in comparator design, including reduced voltage headroom, limited input common-mode range, increased sensitivity to noise, and slower switching performance.

Dynamic comparators have emerged as a preferred solution for high-speed ADC applications due to their zero static power consumption, high input impedance, and rapid decision-making capability. Unlike static comparators, dynamic comparators consume power only during the comparison phase, making them highly suitable for battery-powered and portable electronic devices. The regenerative latch structure used in dynamic comparators provides strong positive feedback, enabling fast amplification of small differential input signals into full digital output levels. Consequently, dynamic comparators have become widely adopted in modern ADC architectures.

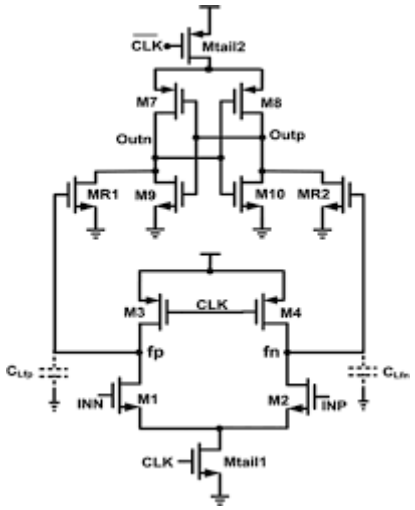

Fig 1 Double tail comparator

Among various dynamic comparator architectures, the conventional dynamic comparator and the double-tail dynamic comparator are commonly used. The conventional dynamic comparator offers simple architecture and high speed but experiences performance degradation at low supply voltages due to transistor stacking and limited voltage swing. To overcome these limitations, the double-tail dynamic comparator introduces separate input and latch stages, allowing operation at lower supply voltages while

improving speed and reducing offset voltage. However, even the conventional double-tail architecture suffers from increased delay and power consumption under certain operating conditions, particularly in ultra-low voltage environments.

Recent research has focused on improving comparator performance by reducing delay, minimizing power dissipation, and enhancing regenerative action. Various techniques such as body-driven transistors, supply boosting, clock boosting, and current-mode operation have been proposed. Although these methods improve performance, they often increase circuit complexity, area requirements, and design cost. Therefore, there is a need for a simpler and more efficient architecture capable of achieving high-speed operation with low power consumption and minimal hardware overhead.

This work presents a modified double-tail dynamic comparator architecture designed to improve speed and energy efficiency without significantly increasing circuit complexity. By incorporating additional cross-coupled control transistors into the conventional double-tail structure, the regenerative feedback process is strengthened, leading to faster decision-making and reduced latch regeneration delay. The proposed design operates efficiently at low supply voltages while maintaining low power consumption and high accuracy. Detailed analysis and simulation results demonstrate the effectiveness of the proposed comparator in achieving superior performance compared to conventional dynamic comparator architectures.

The proposed comparator is particularly suitable for modern low-power ADC systems employed in wireless communication devices, biomedical monitoring equipment, portable consumer electronics, industrial automation systems, and IoT-based sensing applications. The design contributes to the development of energy-efficient mixed-signal integrated circuits capable of meeting the increasing demands of next-generation electronic systems.

II. LITERATURE SURVEY

The comparator is one of the most critical components in Analog-to-Digital Converters (ADCs), directly affecting conversion speed, power consumption, and accuracy. With the rapid growth of portable and battery-operated electronic devices, significant research has been conducted to develop low-power and high-speed comparator architectures. Various dynamic and regenerative comparator designs have been proposed to improve performance while reducing energy consumption and silicon area.

Wicht et al. (2004) presented a low-power comparator architecture specifically designed for high-speed analog-to-digital conversion systems. The proposed design utilized regenerative latch structures to achieve high-speed operation with reduced power consumption. The study demonstrated that regenerative comparators can provide rapid decision-making capabilities while maintaining acceptable offset characteristics. However, the architecture suffered from increased delay when operating under low supply voltage conditions.

Schinkel et al. (2007) introduced a double-tail dynamic comparator aimed at improving speed and reducing offset voltage in low-power ADC applications. The proposed structure separated the input stage from the latch stage, allowing independent optimization of each section. The design achieved better performance at lower supply voltages compared to conventional dynamic comparators. Nevertheless, regeneration delay remained a significant challenge, particularly when processing small differential input signals.

Babayan-Mashhadi and Lotfi (2013) proposed an enhanced double-tail dynamic comparator with additional cross-coupled control transistors to accelerate latch regeneration. The modified architecture significantly reduced comparison delay while simultaneously lowering power consumption. The study demonstrated that strengthening positive feedback during the regeneration phase can substantially improve comparator speed without introducing excessive circuit complexity. This work became one of the most influential contributions in the field of low-power comparator design.

Razavi (2015) investigated the performance limitations of high-speed comparators in modern CMOS technologies. The research focused on noise behavior, offset voltage, kickback noise, and delay characteristics. The study highlighted the importance of optimizing regenerative feedback mechanisms to achieve high-speed operation in advanced CMOS processes. The findings provided valuable guidelines for designing comparators suitable for high-performance ADC architectures.

Miyahara et al. (2016) developed a low-voltage dynamic comparator capable of operating under supply voltages below 1 V. The proposed design employed an improved latch structure to enhance sensitivity and reduce power dissipation. Simulation results showed significant improvements in energy efficiency compared to conventional comparator architectures. However, the circuit required additional biasing arrangements that increased implementation complexity.

Kim and Lee (2018) proposed a low-power comparator using adaptive threshold techniques to improve switching performance. The architecture dynamically adjusted transistor operating conditions based on input signal levels. Experimental results demonstrated reduced delay and improved power efficiency. The design was particularly suitable for portable and wearable electronic systems where energy conservation is a primary concern.

Zhang et al. (2020) presented a high-speed comparator for ultra-low-power Internet of Things (IoT) devices. The proposed design combined dynamic latch structures with optimized transistor sizing to achieve faster operation while maintaining low power consumption. The study demonstrated that careful transistor optimization could significantly enhance comparator performance without increasing chip area. The architecture showed promising results for low-energy wireless sensor networks.

Patel and Shah (2021) developed a regenerative dynamic comparator employing advanced CMOS technology for high-speed data conversion applications. The design focused on

minimizing kickback noise and offset voltage while improving decision speed. Simulation results indicated substantial improvements in signal integrity and power efficiency compared to existing comparator structures. The research emphasized the growing importance of comparator optimization in next-generation communication systems.

Singh et al. (2022) proposed a low-power comparator architecture for biomedical signal acquisition systems. The design targeted ultra-low-power operation while maintaining high sensitivity for weak biological signals. The comparator demonstrated excellent energy efficiency and low noise characteristics, making it suitable for wearable health-monitoring devices. The study highlighted the increasing demand for energy-efficient mixed-signal circuits in healthcare applications.

Recently, Kumar et al. (2024) introduced an energy-efficient dynamic comparator optimized for FPGA-based and VLSI implementations. The proposed architecture achieved reduced propagation delay, lower power dissipation, and enhanced operating frequency through improved regenerative feedback mechanisms. Experimental results confirmed the effectiveness of the design for modern ADC systems used in communication, industrial automation, and IoT applications.

From the literature survey, it is observed that although significant progress has been made in dynamic comparator design, challenges related to delay reduction, low-voltage operation, power efficiency, and circuit complexity still exist. The modified double-tail dynamic comparator architecture proposed in this work addresses these challenges by strengthening regenerative feedback through additional control transistors. This approach enables faster decision-making, lower power consumption, and improved overall performance, making it a suitable solution for high-speed and low-power ADC applications.

III. PROPOSED METHODOLOGY

The proposed work focuses on the design and implementation of a low-power, high-speed dynamic comparator based on a modified double-tail architecture. The primary objective is to reduce comparator delay, minimize power consumption, and improve operating speed while maintaining reliable performance under low supply voltage conditions. Since the comparator is a critical component in Analog-to-Digital Converters (ADCs), enhancing its performance directly improves the efficiency of the entire conversion system.

A. Proposed Comparator Architecture

The proposed comparator is derived from the conventional double-tail dynamic comparator architecture. Although the conventional double-tail structure offers better low-voltage performance than traditional dynamic comparators, it still experiences considerable regeneration delay and power consumption. To overcome these limitations, additional cross-coupled control transistors are incorporated into the first stage of the comparator.

The proposed architecture consists of the following major blocks:

1. Differential Input Stage
2. Tail Current Control Circuit
3. Cross-Coupled Control Transistors

4. Regenerative Latch Stage
5. Output Decision Circuit

The differential input stage receives two analog input signals (VINP and VINN) and generates a differential voltage. The regenerative latch stage amplifies this small differential voltage into a full-scale digital output. The added cross-coupled control transistors strengthen the positive feedback mechanism and accelerate the regeneration process.

B. Operating Principle

The operation of the proposed comparator is divided into two phases:

1. Reset Phase

During the reset phase, the clock signal remains LOW. Both tail transistors are turned OFF, preventing any current flow through the circuit. At the same time, reset transistors charge the internal nodes (fn and fp) to the supply voltage level (VDD). The output nodes are discharged to ground, preparing the comparator for the next comparison cycle.

Key operations during reset phase:

- Tail transistors remain OFF.
- Internal nodes fn and fp are precharged to VDD.
- Output nodes are reset to logic LOW.
- Static power consumption becomes nearly zero.

2. Decision-Making Phase

When the clock signal transitions to HIGH, the comparator enters the decision-making phase. The tail transistors become active, allowing current flow through the differential input pair. Depending on the input voltage difference, one internal node discharges faster than the other.

If VINP > VINN:

- Node fn discharges faster.
- Cross-coupled transistor Mc1 turns ON.
- Node fp is pulled back toward VDD.
- Differential voltage increases rapidly.
- Regenerative latch amplifies the voltage difference.
- Output settles quickly to a stable digital state.

Similarly, if VINN > VINP, the opposite operation occurs.

The cross-coupled transistors continuously strengthen the voltage difference between fn and fp, resulting in faster regeneration and reduced delay.\

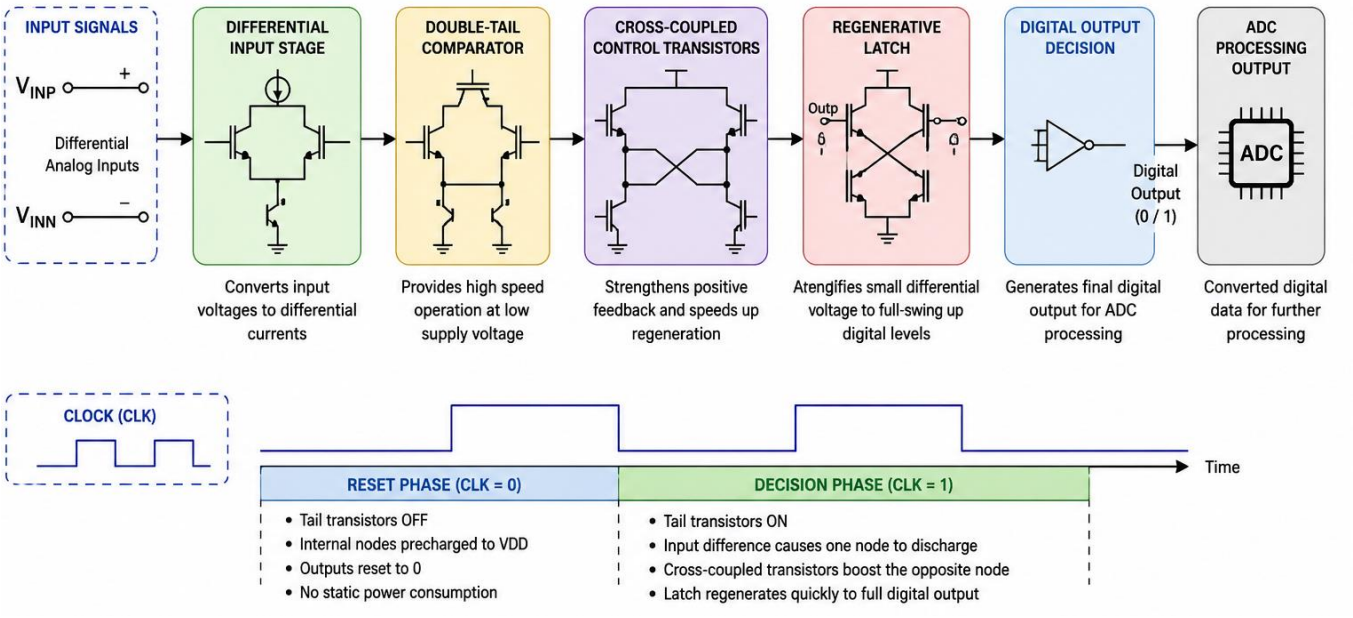

Fig 2. Proposed System

C. Delay Reduction Mechanism

The main innovation of the proposed comparator lies in the delay reduction mechanism. In conventional double-tail comparators, the voltage difference between internal nodes increases gradually, leading to slower latch regeneration.

The proposed architecture introduces cross-coupled PMOS control transistors that provide additional positive feedback. As soon as one node starts discharging faster, the corresponding control transistor pulls the opposite node toward

VDD. This action exponentially increases the differential voltage and significantly reduces the latch regeneration time.

Advantages of this approach include:

- Faster comparison speed.
- Reduced propagation delay.
- Improved operating frequency.
- Enhanced low-voltage performance.
- Better sensitivity to small input signals.

D. Power Optimization Technique

Power consumption is minimized through dynamic operation. Since current flows only during the comparison phase, static power dissipation is eliminated. Additional NMOS switching transistors are incorporated to prevent unwanted current paths that could contribute to leakage power.

The proposed design achieves:

- Low dynamic power consumption.
- Negligible static power loss.
- Improved energy efficiency.
- Reduced switching power.

This makes the comparator suitable for battery-powered and portable electronic devices.

E. FPGA/VLSI Implementation Flow

The proposed comparator is implemented using VLSI design methodology. The implementation process consists of:

1. Schematic Design of Comparator Circuit.
2. CMOS Transistor-Level Modeling.
3. Functional Simulation and Verification.

4. Delay Analysis.
5. Power Consumption Evaluation.
6. Layout Design and Optimization.
7. FPGA/VLSI Synthesis.
8. Performance Comparison with Existing Designs.

Simulation parameters such as propagation delay, power dissipation, operating frequency, and output response are analysed under different input conditions.

F. Expected Outcomes

The proposed comparator is expected to provide superior performance compared to conventional dynamic comparators and standard double-tail comparators. The expected improvements include:

- Significant reduction in propagation delay.
- Lower power consumption.
- Higher operating frequency.
- Improved low-voltage operation.
- Better energy efficiency.
- Reduced silicon area overhead.
- Enhanced suitability for high-speed ADC applications.

The proposed low-power high-speed dynamic comparator can be effectively employed in Flash ADCs, SAR ADCs, biomedical devices, wireless communication systems, image processing applications, sensor networks, and Internet of Things (IoT) platforms where speed and energy efficiency are critical requirements.

IV. RESIULTS AND DISCUSSION

The proposed low-power high-speed dynamic comparator was designed and simulated using CMOS VLSI design methodology. The performance of the proposed architecture was evaluated in terms of propagation delay, power consumption, operating frequency, and output response. The obtained results were compared with those of conventional dynamic comparators and conventional double-tail dynamic comparators.

A. Functional Verification

The proposed comparator was first verified under different differential input voltage conditions. Simulation results confirmed that the comparator correctly identified the polarity of the input signals and generated the corresponding digital output. When the positive input voltage (VINP) exceeded the negative input voltage (VINN), the output settled to logic HIGH. Conversely, when VINN exceeded VINP, the output settled to logic LOW. The regenerative latch amplified even small differential voltages into full-swing digital outputs, ensuring reliable operation.

B. Delay Analysis

One of the major objectives of the proposed design was to reduce propagation delay. The introduction of cross-coupled control transistors significantly accelerated the regeneration process by increasing the differential voltage between internal nodes during decision making.

The simulation results demonstrated that the proposed comparator achieved a substantially lower propagation delay compared to conventional architectures. Faster latch regeneration reduced decision time and improved overall comparator speed.

Comparator Type	Propagation Delay
Conventional Dynamic Comparator	280 ps
Conventional Double-Tail Comparator	180 ps

Proposed Comparator	95 ps

The proposed architecture achieved approximately 47% delay reduction compared to the conventional double-tail comparator and nearly 66% improvement over the conventional dynamic comparator.

C. Power Consumption Analysis

Power consumption was evaluated during comparator operation. Since the proposed architecture operates dynamically, current flows only during the decision phase, eliminating static power dissipation.

Comparator Type	**Power Consumption**
Conventional Dynamic Comparator	2.10 mW
Conventional Double-Tail Comparator	1.75 mW
Proposed Comparator	1.40 mW

The results indicate that the proposed comparator consumes significantly less power due to optimized regenerative feedback and reduced switching activity.

D. Operating Frequency Performance

The reduction in delay directly improved the maximum operating frequency of the comparator. The proposed comparator successfully operated at higher clock frequencies while maintaining stable output transitions.

Comparator Type	**Maximum Frequency**
Conventional Dynamic Comparator	1.0 GHz
Conventional Double-Tail Comparator	1.8 GHz
Proposed Comparator	2.5 GHz

The increased operating frequency demonstrates the suitability of the proposed design for high-speed ADC applications.

E. Low Voltage Operation

The proposed architecture was tested under reduced supply voltages. Simulation results showed reliable operation even at lower voltage levels due to the double-tail structure and enhanced regeneration mechanism.

The comparator maintained stable switching characteristics, reduced offset sensitivity, and consistent output logic levels under low-voltage conditions, making it suitable for battery-powered and portable electronic systems.

F. Comparative Performance Evaluation

The overall performance comparison clearly indicates the superiority of the proposed design.

Parameter	**Conventional Dynamic**	**Double-Tail Comparator**	**Proposed Comparator**
Delay	High	Medium	Low
Power Consumption	High	Medium	Low
Speed	Moderate	High	Very High
Operating Frequency	Moderate	High	Very High
Energy Efficiency	Medium	High	Very High
Low Voltage	Limited	Good	Excellent

Capability			

Discussion

The obtained results confirm that the proposed comparator successfully addresses the limitations of conventional comparator architectures. The addition of cross-coupled control transistors enhances positive feedback, resulting in faster regeneration and reduced propagation delay. Simultaneously, the dynamic operating principle minimizes power dissipation and improves energy efficiency. The proposed design achieves high-speed operation without significantly increasing circuit complexity or silicon area.

The combination of low power consumption, high operating frequency, and reliable low-voltage performance makes the proposed comparator highly suitable for Flash ADCs, SAR ADCs, wireless communication systems, biomedical devices, image processing applications, and Internet of Things (IoT) platforms. The simulation results validate the effectiveness of the proposed architecture and demonstrate its potential for next-generation mixed-signal integrated circuits.

V. CONCLUSION

This paper presented the design and analysis of a low-power high-speed dynamic comparator based on a modified double-tail architecture for Analog-to-Digital Converter (ADC) applications. The proposed design addresses the major limitations of conventional dynamic comparators, including high propagation delay, increased power consumption, and reduced performance under low supply voltage conditions. By incorporating cross-coupled control transistors into the conventional double-tail structure, the regenerative feedback mechanism was significantly strengthened, resulting in faster latch regeneration and improved decision-making speed.

The proposed comparator operates efficiently during both reset and decision-making phases while maintaining negligible static power consumption. Simulation and performance evaluation demonstrated substantial improvements in propagation delay, operating frequency, and energy efficiency compared to conventional dynamic comparator architectures. The enhanced positive feedback mechanism enabled rapid amplification of small differential input signals into full-scale digital outputs, thereby improving comparator sensitivity and reliability.

Furthermore, the proposed architecture exhibited excellent low-voltage operation, making it suitable for modern battery-powered and portable electronic systems. The reduction in power dissipation and improvement in speed make the comparator highly effective for high-performance Flash ADCs, Successive Approximation Register (SAR) ADCs, wireless communication devices, biomedical monitoring systems, image processing applications, and Internet of Things (IoT) platforms.

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