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Research Paper

A THREE-STAGE AMPLIFIER FOR POWERING BIG CAPACITIVE LOADS USING BUFFERED ASYMMETRIC DUAL PATH WITH CASCODE MILLER COMPENSATION

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Abstract: This paper presents a new frequency compensation approach for three-stage amplifiers driving a pF-to-nF capacitive load. Thanks to the cascode Miller compensation, the non-dominant complex pole frequency is extended effectively, and the physical size of the compensation capacitors is also reduced. A local Q-factor control (LQC) loop is introduced to alter the Q-factor adaptively when loading capacitance CL varies significantly. This LQC loop decides how much damping current should be injected into the corresponding parasitic node to control the Q-factor of the complex-pole pair, which affects the frequency peak at the gain plot and the settling time of the proposed amplifier in the closed-loop step response. Additionally, a left-half-plane (LHP) zero is created to increase the phase margin and a feed-forward transconductance stage is paralleled to improve the slew rate (SR). Simulated in 0.13-µm CMOS technology, the amplifier is verified to handle a 4-pF-to-1.5-nF (375× drivability) capacitive load with at least 0.88-MHz gain-bandwidth (GBW) product and 42.3◦ phase margin (PM), while consuming 24.0-µW quiescent power at 1.0-V nominal supply voltage.

INTRODUCTION

The single-stage amplifier used to be one of the strongest candidates for precise analog signal processing when old CMOS technologies were employed because of its high-speed and inherent good stability characteristics. As proved in [1], a single-stage telescopic cascode amplifier can achieve up to 100-dB low-frequency voltage gain with 0.8-µm CMOS technology. However, as the output impedance of the MOSFET is further decreased due to the channel-modulation effect in the modern advanced CMOS technology, it is more difficult for traditional single-stage amplifiers to obtain high voltage gain. In that case, some techniques have been proposed to enlarge the voltage gain of single-stage amplifiers, such as output resistance boosting, transconductance (Gm) boosting and multiple small-gain stages cascading [2–4]. In these strategies, stability, output swing and power efficiency are always traded for voltage gain. More importantly, most of them cannot deliver the required high voltage gain (>100 dB) for the high accuracy applications requiring precision buffering. Cascading multiple gain stages is a good way to get high voltage gain because it is potentially power-efficient with low supply voltage. One of the essential problems for multistage amplifiers is theclosed-loop stability. Generally speaking, there are at least three poles that exist in the transfer function of the loop gain of a three-stage amplifier. If the poles and zeros were distributed inappropriately, the multistage amplifier would encounter a closed-loop stability issue [5]. As to the stability criteria, it normally can be indicated by the parameters of phase margin (PM) or gain margin (GM) in the Bode plot for the design of single-stage and two-stage amplifiers. However, the stability analysis of multistage amplifiers is more complex than single- or two-stage amplifiers due to the existence of complex poles in high-order transfer functions [6]. Moreover, the key specifications (e.g., gain-bandwidth (GBW), PM, GM) are normally tied to the frequency compensation approach and the value of the capacitive load CL. Several compensation schemes for three-stage amplifiers have been reported in the past few decades [7–19]. Nested-Miller compensation (NMC) is known as one of the most classical pole-splitting techniques for three-stage amplifiers frequency compensation. The basic idea of NMC scheme is to capacitively nest several pairs of gain stages to achieve pole-splitting [7]. However, the bandwidth reduction, which is mainly caused by the required large value Miller capacitor, degrades the benefits of the technique. To tackle this problem, other compensation schemes based on NMC have been proposed [8–14], some of which could enlarge the GBW tenfold comparing with the traditional NMC technique. Generally, they either removed the inner Miller capacitor or replaced the outer compensation loop with more advanced compensation techniques [11,15–17] to extend complex-pole frequency ωo. In some others designs, like [20] and [21], either an active zero or a wide-bandwidth scalar is embedded in the multistage amplifier to extend the non-dominant pole frequency for driving an extremely large capacitive load. Naturally, these techniques can achieve better small-signal performance by increasing the product of load capacitor value and unit-gain frequency. These techniques, however, fail to tackle the problem of frequency peak at gain plot due to a large Q-factor of complex-pole when the load capacitance is dropped significantly [22]. As a result, in the transient step response, a high-frequency oscillation would appear and last for a long period [17]. Most existing frequency compensation schemes for three-stage amplifiers focus on maximizing the performance for a single value of capacitive load CL (especially the large CL) to achieve better figure-of-merit (FOM) rather than extending the drivability range of CL. However, the load capacitance can change in the range of pF–nF depending on applications such as headphone, liquid-crystal display (LCD) or microelectromechanical systems (MEMS) capacitive sensors [23–25]. In other words, an amplifier with wide capacitive loading drivability can find more applications and is easy to be reused in a different environment. As a result, there is no need to design the amplifier circuits case by case when the loading capacitance is different, which is helpful to shorten the design procedure and save the production cost. The technique for extending the drivability range of two-stage amplifiers has been studied in [26]. Comparing with the two-stage amplifiers, it is more difficult to stabilize and even more challenging to extend the drivability range for three-stage amplifiers. Although some three-stage amplifiers with wide bandwidth have been reported to have large driving capability for large capacitive load [21,27], it is hard to find amplifier designs able to combine the possibility to drive capacitive load in the pF and nF range with low quiescent power and small active area [28–30]. Expanding the report in [31], this paper provides the analysis and design insights for a low-power three-stage amplifier capable of driving the pF-to-nF capacitive load. The cascode Miller compensation in the outer feedback loop helps to extend the non-dominant complex-pole frequency and the physical size of the compensation capacitors is reduced as well. The Q-factor of the complex-pole pair is controlled by the local feedback loop adaptively, which improves the frequency response and shortens the transient settling time. In this design, 375× capacitive load drivability is realized for the proposed amplifier. Additionally, at least 0.88-MHz GBW and 0.41-V/µs average slew rate (SR) of the proposed three-stage amplifiers are achieved with 24.0-µW power consumption.

II.LITERATURE SURVEY:

A 100-MHz 100-dB operational amplifier with multipath nested Miller compensation structure

A 100-MHz bipolar operational amplifier has a gain of 100 dB. The op amp owes its high unity-gain bandwidth and high gain to an all-n-p-n signal path and multipath nested Miller compensation (MNMC). The phase margin with a 100-pF load is 40 degrees at 100 MHz and the amplifier settles in 60 ns to 0.1% on a 1-V step. For comparison, a similar op amp without the multipath technique has been realized. The unity-gain bandwidth of this nested Miller compensation (NMC) op amp is 60 MHz and the settling time is 70 ns. Theory and measurements confirm that the multipath technique almost doubles the bandwidth of nested Miller compensated amplifiers.

Active-feedback frequency-compensation technique for low-power multistage amplifiers

An active-feedback frequency-compensation (AFFC) technique for low-power operational amplifiers is presented in this paper. With an active-feedback mechanism, a high-speed block separates the low-frequency high-gain path and high-frequency signal path such that high gain and wide bandwidth can be achieved simultaneously in the AFFC amplifier. The gain stage in the active-feedback network also reduces the size of the compensation capacitors such that the overall chip area of the amplifier becomes smaller and the slew rate is improved. Furthermore, the presence of a left-half-plane zero in the proposed AFFC topology improves the stability and settling behavior of the amplifier. Three-stage amplifiers based on AFFC and nested-Miller compensation (NMC) techniques have been implemented by a commercial 0.8-µm CMOS process. When driving a 120-pF capacitive load, the AFFC amplifier achieves over 100-dB dc gain, 4.5-MHz gain-bandwidth product (GBW) , 65° phase margin, and 1.5-V/µs average slew rate, while only dissipating 400-µW power at a 2-V supply. Compared to a three-stage NMC amplifier, the proposed AFFC amplifier provides improvement in both the GBW and slew rate by 11 times and reduces the chip area by 2.3 times without significant increase in the power consumption.

Dual Active-Capacitive-Feedback Compensation for Low-Power Large-Capacitive-Load Three-Stage Amplifiers

A dual active-capacitive-feedback compensation (DACFC) scheme for low-power three-stage amplifiers with large capacitive loads is presented in this paper. Dual high-speed active-capacitive-feedback paths enable the non-dominant complex poles of the amplifier to be located at high frequencies for bandwidth extension under low-power condition. The proposed DACFC amplifier also consists of two left-half-plane (LHP) zeros that relax the stability criteria for further improving the gain-bandwidth product (GBW) and reducing the required compensation capacitance of the amplifier. Moreover, the transient response of the DACFC amplifier is enhanced via the use of the small compensation capacitance and the presence of push-pull second and output stages.

A 0.016-mm2 144-µ W Three-Stage Amplifier Capable of Driving 1-to-15 nF Capacitive Load With >0.95-MHz GBW

A 0.016-mm^2 144-µ W three-stage amplifier capable of driving 1-to-15-nF capacitive load (C_L) is described. It is optimized via combining current-buffer Miller compensation and parasitic-pole cancellation (via an active left-half-plane zero circuit) to extend the C_L drivability with small power and area. Fabricated in 0.35-µ m CMOS, the minimum gain-bandwidth product (GBW), slew rate (SR) and phase margin measured over 1-to-15-nF C_L are 0.95 MHz, 0.22 V/ µs and 52.3 °, respectively. The results at 15-nF C_L correspond to 2.02x-improved small-signal FOM_S (=GBW·C_L/Power), and 1.44x-improved large-signal FOM_L (=SR·C_L/Power) with respect to prior art. The sizing and optimization are systematically guided by Local Feedback Loop Analysis. It is an insightful control-centric method allowing the pole-zero placements to be more analyzable and comparable at the system level.

Design-Oriented Analysis for Miller Compensation and Its Application to Multistage Amplifier Design

A design-oriented analysis (DOA) method is presented, which lends sufficient insights into various Miller compensation schemes. The method predicts the nondominant poles of the Miller-compensated amplifiers in an intuitive manner, and it serves as a good supplement to the conventional analysis. The usage of DOA is verified by the various design examples given in this paper. Guided by DOA, a multistage amplifier capable of driving a large-capacitive load (CL) with low power consumption is presented. This amplifier employs an active zero to extend its Miller loop bandwidth, thereby pushing the amplifier's nondominant poles to high frequencies and achieving larger gain bandwidth (GBW). Fabricated in a 0.18-µm CMOS process, the amplifier achieves 1.18-MHz GBW and 59.6° phase margin when driving an 18-nF CL , while consuming 69.6 µW from a 1.2-V supply. The design shows improved figures-of-merit compared with the prior state-of-the-art Miller-compensated multistage amplifiers.

Enhanced active-feedback frequency compensation with on-chip-capacitor reduction feature for amplifiers with large capacitive load

A large capacitive load amplifier with enhanced active-feedback frequency compensation is proposed in this paper. The enhancement is achieved through using a wide-bandwidth scalar circuit to increase the transconductance of the output stage so that the overall bandwidth of the amplifier can be extended considerably. Implemented in a standard CMOS 130-nm technology, with a supply of 0.7 V and consuming 27 µA of current, the amplifier drives a load capacitor of 15 nF. No on-chip resistor is needed; only a 0.91-pF compensation capacitor is used to maintain stability. The achieved gain-bandwidth product and phase margin are 1.28 MHz and 66.9°, respectively. Moreover, the slew rate is 0.263 V/µs. The active chip area is 0.0056 mm^2.

III.PROPOSED CASCODE MILLER-COMPENSATION WITH LOCAL Q-FACTOR CONTROL (CLQC)

As mentioned in previous sections, a high Q-factor could result in unstable amplifiers if CL is reduced or increased significantly according to different design topologies. The idea of the proposed work is to design an advanced compensation topology that can control the Q-factor of the complex pair in a proper range when CL changes significantly. 3.1. Structure Figure 4 shows the equivalent diagram of the proposed three-stage cascode Miller-compensation with local Q-factor control (CLQC) amplifier [31]. It consists of two inverting gain stages, a non-inverting gain stage, two current buffered Miller compensation blocks, and one feed-forward block. Like [16], the cascode Miller compensation block (+Gma1 and Cm1) eliminates the feed-forward signal path (which may cause the right-half-plane (RHP) zero) that exists in simple Miller compensation, creates an LHP (left half-plane) zero and extends the complex-pole frequency. A feed-forward path (Gmf) is added to form a push-pull output stage with GmL to improve the transient performance. Unlike the realization in [15], the other local Miller compensation block (–Gma2 and Cm2) is not aimed at creating an LHP zero for pole-zero cancellation but composing a local Q-factor control loop with the second gain stage. It controls the amount of damping current to be injected in Cm2 to alter the small-signal impedance at the output node of Gm2 (v3 in Figure 4), which affects the Q-factor of the corresponding complex-pole.

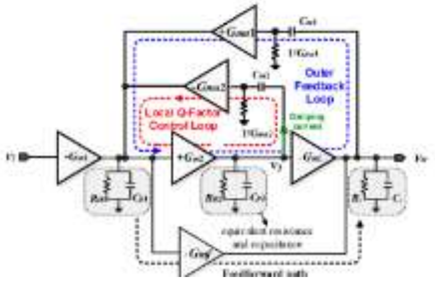


Figure 1. Equivalent diagram of the proposed three-stage cascode Miller-compensation with local Q-factor control (CLQC) amplifier.

Small-Signal Analysis of the Proposed Three-Stage CLQC Amplifier

The equivalent small-signal model of the proposed three-stage CLQC amplifier is shown in Figure 5, where Gmi, Roi, and Cpi are noted as the equivalent transconductance, output resistance and the lumped capacitance at the ith gain stage, Gma1 and Gma2 are the equivalent transconductances of the current buffered Miller compensation stages, and Gmf is the feed-forward transconductance.

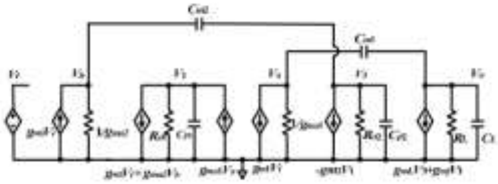


Figure 2. The equivalent small-signal model of the proposed three-stage CLQC amplifier.

Circuit Implementation

The schematic of the proposed three-stage amplifier with CLQC technique is depicted in Figure 8 [31]. The 1st stage uses a folded cascode structure (M1–M9). The 2nd stage adopts a current mirror to form the non-inverting stage (M10–M14). Assuming the transconductance of M11, M12 and M13 are gm2,1, gm2,2 and gm2,3, respectively, the overall transconductance gm2 is, therefore (gm2,1*gm2,3)/gm2,2. The 3rd stage is formed by a common-source stage (M16). The cascode Miller compensation is realized by Cm1 and the common-gate stage (M7). The local Q-factor control block contains Miller capacitor Cm2 and the common-source stage (M9). The NMOS transistor M15 generates a feed-forward path, which is helpful to enhance the transient performance. The quiescent current of the amplifier core circuit for each branch is labeled properly in Figure 8. As to optimize the compensation capacitor value of the proposed CLQC amplifier, the value of Cm1 and Cm2 are set to be 1 and 0.05 pF, respectively, for the extreme capacitive load ranging from 4 pF to 1.5 nF. The purpose of this design is to extend the loading capacitive range with low power consumption and wide bandwidth by comparing with the state-of-the-arts [8–10].

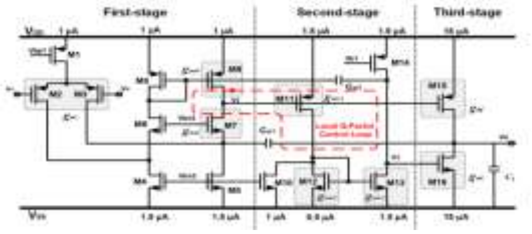
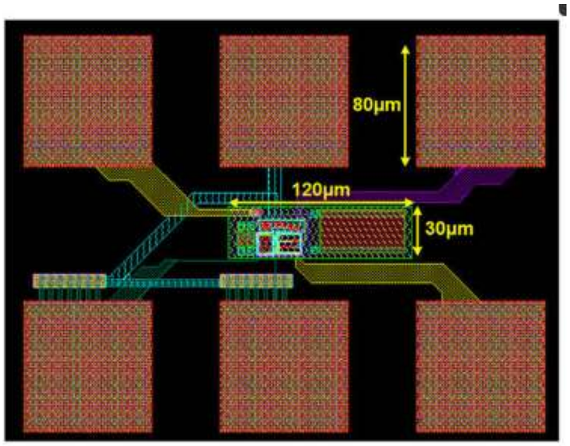


Figure 3. The simplified schematic of the proposed three-stage CLQC amplifier.

IV.SIMULATION RESULTS:



V.CONCLUSION

In this paper, a low-power (24.0-μW) three-stage CMOS amplifier with 375x capacitive load (CL) drivability range is presented. Combining cascode and Miller compensation, the complex-pole frequency ωo is extended effectively which enables higher GBW of the proposed amplifier. Pushing the complex-pole to higher frequency while lowering its Q-factor are a contradiction as studied in prior designs. Thanks to the proposed CLQC technique, the Q-factor of the complex poles is restricted to an appropriate range while the complex-pole frequency ωo is maintained according to different CL applied at the output. Therefore, an optimized tradeoff between complex-pole frequency ωo and the Q-factor is achieved. The proposed amplifier was verified by 0.13-μm CMOS technology, and the simulation results show at least 0.88-MHz GBW and 0.41 V/μs average are achieved under 4-pF-to-1.5-nF CL, and the on-chip compensative capacitance is only 1.05 pF.

References

1. Gulati, K.; Lee, H.S. A high-swing CMOS telescopic operational amplifier. IEEE J. Solid-State Circuits 1998, 33, 2010–2019. [CrossRef]

2. Sackinger, E.; Guggenbuhl, W. A high-swing, high-impedance MOS cascode circuit. IEEE J. Solid-State Circuits 1990, 25, 289–29

3. Li, Y.L.; Han, K.F.; Tan, X.; Yan, N.; Min, H. Transconductance enhancement method for operational transconductance amplifiers. Electron. Lett. 2010, 46, 1321–1323. [CrossRef]

4. Ho, M.; Leung, K.N.; Mak, K.L. A low-power fast-transient 90-nm low-dropout regulator with multiple small-gain stages. IEEE J. Solid-State Circuits 2010, 45, 2466–2475. [CrossRef]

5. Cheng, Q.; Zhang, H.; Xue, L.; Guo, J. A 1.2-V 43.2-μW three-stage amplifier with cascode Miller-compensation and Q-reduction for driving large capacitive load. In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), Montreal, QC, Canada, 22–25 May 2016; pp. 458–461.

6. Nguyen, R.; Murmann, B. The design of fast-settling three-stage amplifiers using the open-loop damping factor as a design parameter. IEEE Trans. Circuits Syst. I Reg. Papers 2010, 57, 1244–1254. [CrossRef]

7. Eschauzier, R.G.H.; Kerklaan, L.P.T.; Huijsing, J.H. A 100-MHz 100-dB operational amplifier with multipath nested Miller compensation structure. IEEE J. Solid-State Circuits 1992, 27, 1709–1717. [CrossRef]

8. Leung, K.N.; Mok, P.K.T. Analysis of multistage amplifier - frequency compensation. IEEE Trans. Circuits Syst. I Reg. Papers 2001, 48, 1041–1056. [CrossRef]

9. You, F.; Embabi, S.H.K.; Sanchez-Sinencio, E. Multistage amplifier topologies with nested Gm-C compensation. IEEE J. Solid-State Circuits 1997, 32, 2000–2010. [CrossRef]

10. Leung, K.N.; Mok, P.K.T.; Ki, W.H.; Sin, J.K.O. Three-stage large capacitive load amplifier with damping-factor-control frequency compensation. IEEE J. Solid-State Circuits 2000, 35, 221–230. [CrossRef]

11. Lee, H.; Mok, P.K.T. Active-feedback frequency-compensation technique for low-power multistage amplifiers. IEEE J. Solid-State Circuits 2003, 38, 511–520. [CrossRef] 12. Peng, X.; Sansen, W. AC boosting compensation scheme for low power multistage amplifiers. IEEE J. Solid-State Circuits 2004, 39, 2074–2079. [CrossRef]

13. Fan, X.; Mishra, C.; Sanchez-Sinencio, E. Single Miller capacitor frequency compensation technique for low-power multistage amplifiers. IEEE J. Solid-State Circuits 2005, 40, 584–592.

14. Peng, X.; Sansen, W.; Hou, L.; Wang, J.; Wu, W. Impedance adapting compensation for low-power multistage amplifiers. IEEE J. Solid-State Circuits 2011, 46, 445–451. [CrossRef]

15. Guo, S.; Lee, H. Dual active-capacitive-feedback compensation for low-power large-capacitive-load three-stage amplifiers. IEEE J. Solid-State Circuits 2011, 46, 452–464. [CrossRef]

16. Chong, S.S.; Chan, P.K. Cross feedforward cascode compensation for low-power three-stage amplifier with large capacitive load. IEEE J. Solid-State Circuits 2012, 47, 2227–2234. [CrossRef]

17. Yan, Z.; Mak, P.I.; Law, M.-K.; Martins, R.P. A 0.016 mm2 144 μW three-stage amplifier capable of driving 1-to-15 nF capacitive load with 0.95 MHz GBW. IEEE J. Solid-State Circuits 2013, 48, 527–540. [CrossRef]

18. Qu, W.; I'm, J.-P.; Kim, H.-S.; Cho, G.-H. A 0.9V 6.3μW multistage amplifier

driving 500 pF capacitive load with 1.34MHz GBW. In Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 9–13 February 2014; pp. 290–292.

19. Yan, Z.; Mak, P.I.; Law, M.-K.; Martins, R.P. A 0.0013 mm2 3.6 µW nested-current-mirror single-stage amplifier driving 0.15-to-15 nF capacitive loads with >62◦ phase margin. In Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 9–13 February 2014; pp. 288–289.

20. Qu, W.; Singh, S.; Lee, Y.; Son, Y.; Cho, G. Design-oriented analysis for Miller compensation and its application to multistage amplifier design. IEEE J. Solid-State Circuits 2017, 52, 517–527. [CrossRef]