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Research Paper

Optimization Using Braun Multiplier and Ripple Carry Adder (RCA)

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ABSTRACT

This project presents the design and implementation of a Finite Impulse Response (FIR) filter using a Braun Multiplier and Ripple Carry Adder (RCA) for efficient digital signal processing applications. FIR filters are widely used in communication, audio processing, biomedical systems, and image enhancement because of their stability and linear phase characteristics. In this work, the Braun multiplier is used for multiplication operations due to its regular structure and area efficiency, while the RCA is utilized for accumulation because of its simplicity and low hardware complexity. The complete architecture is modeled using Verilog HDL and simulated using Xilinx ISE for functional verification and synthesis. The proposed design achieves reliable filtering performance with acceptable area utilization and moderate speed. Although the RCA introduces propagation delay, the architecture remains suitable for low-cost and low-power applications. Simulation results confirm correct signal processing behavior with stable output characteristics. The design provides a strong foundation for future optimization using advanced high-speed arithmetic units. Overall, the project demonstrates a balanced trade-off between hardware efficiency, simplicity, and computational accuracy in FIR filter implementation.

Keywords: FIR Filter, Braun Multiplier, Ripple Carry Adder, Verilog HDL, Digital Signal Processing, Xilinx ISE, VLSI Design, Area Efficiency, Signal Filtering.

INTRODUCTION

Finite Impulse Response (FIR) filters are among the most important components used in Digital Signal Processing (DSP)

systems. They are widely utilized in applications such as communication systems, biomedical instrumentation, image processing, radar systems, and audio enhancement. FIR filters are preferred because they provide inherent stability and linear phase response, ensuring predictable and distortion-free signal processing. Unlike IIR filters, FIR filters depend only on present and past input values, avoiding feedback and maintaining stable operation.

The performance of FIR filters mainly depends on the efficiency of arithmetic units such as multipliers and adders. Multipliers are responsible for generating partial products using filter coefficients, while adders accumulate these products to form the final output. In this project, a Braun Multiplier and Ripple Carry Adder (RCA) are used to implement the FIR filter architecture. The Braun multiplier offers a regular array structure suitable for VLSI implementation and provides moderate speed with reduced hardware complexity. The Ripple Carry Adder performs binary addition sequentially and is easy to implement with low area consumption.

The proposed design is modeled using Verilog HDL and verified using Xilinx ISE simulation tools. The architecture aims to achieve an effective balance between area efficiency, simplicity, and functional accuracy. Although the RCA introduces carry propagation delay, the design remains suitable for low-cost DSP applications. This project also provides a platform for future research using high-speed adder structures and advanced multiplier architectures for improved performance.

LITERATURE SURVEY

Several researchers have proposed different FIR filter architectures to improve speed, power efficiency, and area optimization. P. Ramesh et al. designed an FIR filter using a Vedic multiplier to reduce propagation delay and improve processing speed. Their design achieved better performance compared to conventional multipliers while maintaining low area utilization. M. Kumar and his team introduced a low-power FIR filter using a Modified Booth multiplier and Carry Look Ahead Adder, which significantly improved speed and reduced power consumption.

T. Venkatesh proposed FPGA implementation techniques using parallel processing architectures for increasing FIR filter throughput. Another study by R. Anitha utilized a Wallace Tree multiplier with Ripple Carry Adder to achieve high-speed filtering performance. D. Lakshmi focused on area-efficient FIR filter implementation using Braun multipliers and RCA structures suitable for low-cost applications. N. Sharma combined Braun

multipliers with Carry Select Adders to improve execution speed and overall efficiency. S. Thomas introduced Distributed Arithmetic-based FIR filters that removed explicit multipliers to reduce power consumption. P. Mahesh implemented clock gating techniques for reducing dynamic power in FIR filters. Comparative studies by L. Banerjee analyzed Braun, Booth, and Wallace multipliers for performance evaluation. S. Reddy demonstrated FPGA-based FIR filters using RCAs for simple and reliable DSP applications. These studies collectively highlight the importance of optimized arithmetic units in FIR filter implementation and motivate the proposed architecture.

EXISTING SYSTEM

Existing FIR filter systems generally use conventional multiplier and adder architectures for signal processing operations. Many traditional FIR filters employ simple array multipliers and Ripple Carry Adders due to their ease of implementation and low hardware complexity. However, these systems suffer from higher propagation delay because carries propagate sequentially from one stage to another.

Conventional architectures also consume more power when operating at high frequencies. In some designs, the hardware area increases significantly due to inefficient multiplier structures. Existing systems may not provide sufficient speed for real-time DSP applications. Additionally, older FIR architectures often lack optimization for VLSI implementations. Though the designs maintain functional accuracy, they experience limitations in throughput and latency. These drawbacks motivate the need for improved architectures with better area efficiency and enhanced computational performance.

PROPOSED SYSTEM

The proposed system implements an FIR filter using a Braun Multiplier and Ripple Carry Adder architecture. The Braun multiplier is selected because of its regular array structure, simple layout, and suitability for VLSI implementation. The Ripple Carry Adder is used for accumulating partial products generated by the multiplier stages. The entire system is modeled using Verilog HDL to achieve accurate hardware representation and easy synthesis.

Xilinx ISE tools are utilized for simulation and verification of the design. The proposed architecture achieves area efficiency while maintaining stable signal processing performance. The design also ensures

simplicity in routing and debugging because of the regular structure of the Braun multiplier. Although the RCA introduces moderate delay, the architecture remains suitable for low-cost and low-power DSP applications. The system provides reliable output with linear phase characteristics and stable filtering behavior. This architecture can further be enhanced using advanced high-speed adders in future implementations.

SYSTEM ARCHITECTURE

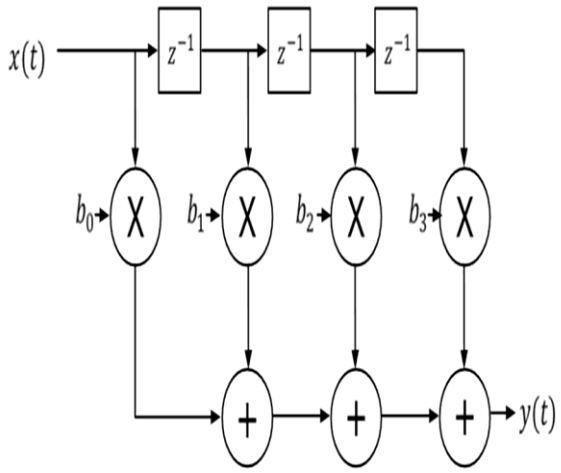


Fig:1 System Architecture

The proposed FIR filter architecture consists of delay elements, Braun multipliers, and Ripple Carry Adders connected in a structured manner. The input signal is passed through a sequence of delay stages to generate delayed versions of the input samples. Each delayed sample is multiplied by predefined filter coefficients using Braun multipliers. These multipliers generate partial products efficiently through parallel operations. The outputs from the multiplier blocks are accumulated using Ripple Carry Adders. The RCA performs sequential binary addition to produce the final filtered output signal. The architecture follows the Direct Form FIR structure commonly used in DSP systems. Verilog HDL is used to describe the structural and behavioral operations of the design. Simulation and synthesis are performed using Xilinx ISE tools for performance verification. The architecture provides an effective balance between hardware simplicity, area utilization, and computational accuracy.

METHODOLOGY DESCRIPTION

The methodology of the proposed FIR filter implementation begins with designing the filter structure using Verilog HDL. First, the FIR filter coefficients are selected according to the required filtering operation. The input signal samples are passed through delay elements to generate multiple delayed versions of the signal. These delayed signals are multiplied with corresponding filter coefficients using Braun multipliers. The Braun multiplier performs multiplication using a parallel array structure that efficiently generates partial products.

The generated products are accumulated using Ripple Carry Adders to produce the final filter output. The RCA performs addition by propagating carries sequentially from the least significant bit to the most significant bit. After coding the architecture in Verilog HDL, simulation is carried out using Xilinx ISE tools. Functional verification ensures that the output response matches the expected filtering behavior. Synthesis analysis is then performed to evaluate area utilization, delay, and hardware efficiency. The architecture is tested using different input conditions to validate stability and reliability. Results obtained from the simulations confirm accurate signal processing with minimal distortion.

The methodology demonstrates an effective balance between computational accuracy and hardware simplicity. The design also supports scalability for higher-order FIR filter implementations. Future optimization can be achieved by replacing the RCA with high-speed adders such as CLA or Kogge-Stone adders.

RESULTS AND DISCUSSION

Simulation and synthesis results confirm the successful implementation of the FIR filter using the Braun multiplier and Ripple Carry Adder architecture. The design was tested using Verilog HDL simulation in Xilinx ISE tools. Results indicate that the FIR filter accurately processes input signals and produces stable outputs with minimal distortion. The Braun multiplier provides efficient multiplication with moderate hardware utilization. The Ripple Carry Adder contributes to reduced circuit complexity and area efficiency. However, the sequential carry propagation introduces moderate delay in the system.

Despite this limitation, the architecture performs reliably for low-speed DSP applications. The overall design achieves a balanced trade-off between area, speed, and implementation complexity.

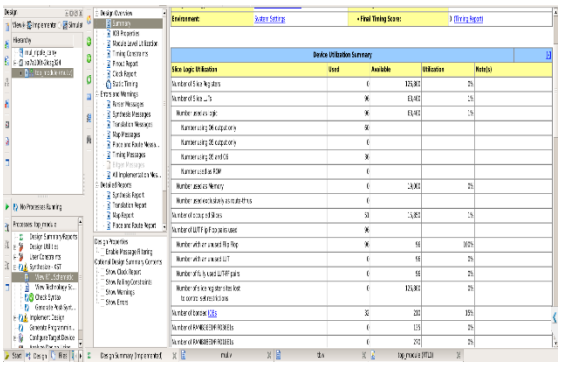


Fig 2: Area

The Braun Multiplier provides a regular and compact hardware structure, resulting in efficient area utilization for FIR filter implementation.

The Ripple Carry Adder (RCA) further reduces hardware complexity, making the overall design suitable for low-area and cost-sensitive applications.

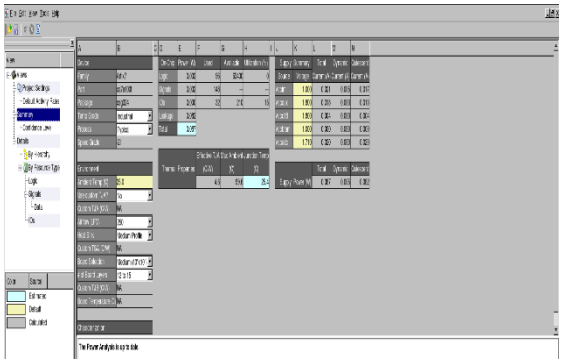


Fig 3: Power Consumption

The proposed FIR filter consumes moderate power due to the simple architecture of the Braun Multiplier and RCA. Reduced hardware resources and regular circuit structure help minimize overall power consumption in DSP applications.

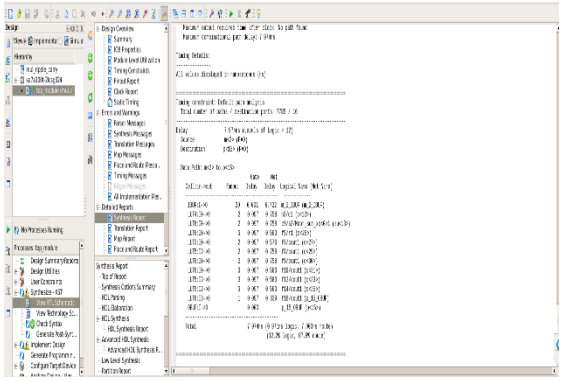


Fig 4: Delay

The RCA introduces propagation delay because carries are transferred sequentially from the least significant bit to the most significant bit. Although the Braun Multiplier performs multiplication efficiently, the overall speed is moderate due to the carry propagation delay of the RCA.

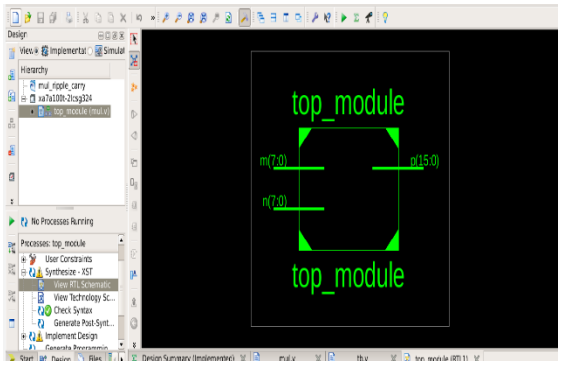


Fig 5: RTL view

The RTL View shows the top-level architecture of the FIR filter including delay elements, Braun Multipliers, Ripple Carry Adders, input signals, and output connections. It represents the data flow between registers and arithmetic blocks, enabling functional verification before synthesis.



Fig 6: Internal RTL view

The Internal RTL View illustrates the detailed implementation of individual modules such as the Braun Multiplier and Ripple Carry Adder. It displays internal logic components, signal paths, and interconnections used to perform

multiplication and accumulation operations within the FIR filter.

WAVEFORM SIMULATION OUTPUT

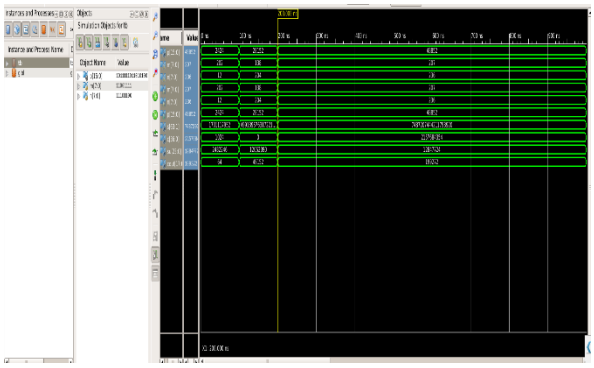


Fig 5: Waveform Simulation

The waveform simulation verifies the functional behavior of the FIR filter by displaying input, intermediate, and output signals over time. It confirms the correct operation of the Braun Multiplier and Ripple Carry Adder by showing accurate multiplication and accumulation results for different input test vectors. The simulation helps identify timing relationships between signals, ensuring that the filter output matches the expected convolution operation.

CONCLUSION

This project successfully demonstrates the design and implementation of an FIR filter using a Braun Multiplier and Ripple Carry Adder. The proposed architecture achieves reliable signal processing performance while maintaining hardware simplicity and area efficiency. The Braun multiplier provides a regular and compact structure suitable for VLSI implementation. The Ripple Carry Adder offers low hardware complexity and ease of implementation. Verilog HDL is effectively used for modeling and simulation of the complete architecture. Functional verification using Xilinx ISE confirms correct operation of the FIR filter. The system maintains stable output characteristics and linear phase response during signal processing. Although the RCA introduces propagation delay, the architecture remains suitable for low-cost and low-power applications. The project establishes a strong foundation for future optimization using advanced arithmetic structures. Overall, the design demonstrates an efficient and practical approach for FIR filter implementation in digital signal processing systems.

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