FPGA-BASED DIGITAL COMMUNICATION SYSTEMS: ARCHITECTURES, APPLICATIONS, AND EMERGING TRENDS

[1] M Swetha, [2] Ruchi Ch, [3] Dr. Vrijesh Kumar Pandey
[1] M. Tech -Communication Systems, MUIT-Lucknow
[2] M. Tech-Communication Systems, MUIT-Lucknow
[3]Professor, MUIT-Lucknow
swetha.m454@gmail.com , ruchi_ch@gmail.com, vrijeshkumar.p@gmail.com

Abstract

Field-Programmable Gate Arrays (FPGAs) have emerged as a pivotal hardware platform for implementing digital communication systems, combining the flexibility of programmable logic with near-ASIC performance. As communication standards grow in complexity—driven by the demands of 5G New Radio, Internet of Things (IoT), and Software-Defined Radio (SDR)—FPGAs provide a reconfigurable, high-throughput substrate that bridges the gap between general-purpose processors and fixed-function ASICs. This paper examines the role of FPGAs in modern digital communication systems, covering fundamental FPGA architectures, modulation and demodulation implementations, error correction coding schemes such as Low-Density Parity-Check (LDPC) and turbo codes, and OFDM-based multi-carrier techniques. The paper also reviews FPGA applications in MIMO transceivers, Software-Defined Radio platforms, and cognitive radio systems. Key performance metrics—including resource utilization, latency, throughput, and power consumption—are discussed alongside implementation challenges such as fixed-point precision, design complexity, and verification overhead. Comparative analysis against DSP processors and ASICs is presented to delineate appropriate use cases for FPGA deployment. The paper concludes with recommendations and directions for future research at the intersection of FPGAs, machine learning, and next-generation communication standards.

***Keywords*:** FPGA, Digital Communications, OFDM, MIMO, LDPC Codes, Software-Defined Radio, 5G, Signal Processing, Reconfigurable Hardware

1. Introduction

Modern digital communication systems demand unprecedented levels of computational throughput, low latency, energy efficiency, and adaptability to evolving wireless standards. From cellular base stations implementing 5G New Radio (NR) to satellite modems and tactical military radios, the physical layer of a communication link must execute complex signal processing functions—modulation, channel coding, equalization, synchronization—in real time and with deterministic timing. These requirements place considerable strain on conventional software-based processing platforms such as general-purpose CPUs and even specialized Digital Signal Processors (DSPs).

Field-Programmable Gate Arrays (FPGAs) have steadily established themselves as a preferred hardware substrate for digital communication prototyping and deployment. Unlike ASICs, which are fabricated for a fixed function and require lengthy development cycles, FPGAs can be configured and reconfigured after manufacturing using Hardware Description Languages (HDLs) such as VHDL or Verilog, or increasingly through High-Level Synthesis (HLS) tools. This reconfigurability enables engineers to rapidly iterate designs, update fielded systems via firmware upgrades and support multiple communication standards on a single hardware platform.

The convergence of several technological trends has amplified the relevance of FPGAs in communications research and deployment. The proliferation of Software-Defined Radio (SDR) architectures demands flexible, high-bandwidth baseband processors capable of implementing diverse waveforms without hardware replacement. The adoption of Orthogonal Frequency Division Multiplexing (OFDM) in standards such as LTE, IEEE 802.11, and 5G NR requires high-parallelism Fast Fourier Transform (FFT) engines that FPGAs can implement with low latency and high efficiency. Meanwhile, massive MIMO systems—employing tens to hundreds of antenna elements—require real-time matrix computations that benefit greatly from the spatial parallelism inherent in FPGA logic fabric.

This paper provides a comprehensive survey of FPGA-based digital communication systems. Section 2 reviews the relevant literature on FPGA architectures and communication applications. Section 3 presents the theoretical framework guiding the analysis. Section 4 describes the methodology. Section 5 analyses key implementation examples and discusses performance trade-offs. Section 6 concludes with recommendations for practitioners and researchers. The research objectives are: (i) to characterize FPGA hardware resources and their suitability for communication DSP; (ii) to review FPGA implementations of OFDM, MIMO, and FEC coding; (iii) to evaluate FPGA performance relative to DSP and ASIC alternatives; and (iv) to identify open challenges and emerging research directions.

2. Literature Review

2.1 FPGA Architecture and Resources

An FPGA is an integrated circuit consisting of an array of programmable logic blocks—typically Look-Up Tables (LUTs), flip-flops, and carry chains—interconnected through a hierarchy of configurable routing resources. Modern high-end devices from Xilinx (now AMD) and Intel (formerly Altera) supplement the reconfigurable logic fabric with dedicated resources that are particularly valuable for signal processing: hardened DSP slices implementing high-speed multiply-accumulate (MAC) operations, block RAMs for on-chip data buffering, high-speed serial transceivers (GTX/GTP/GTH) for line rates exceeding 10 Gbps, and embedded processor cores (ARM Cortex-A53/A72 in Zynq Ultra Scale+ devices) for control-plane processing.

The ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2024) highlighted novel hardware/software co-design and high-level synthesis methodologies enabling digital signal processing, compute acceleration, and networking as among the most active research areas in the FPGA community. The symposium noted that FPGA technology has become more crucial than ever for delivering the energy efficiency and low latency demanded by communications and AI applications. These observations reflect a broader trend: modern FPGAs are no longer purely reconfigurable logic devices but heterogeneous System-on-Chip (SoC) platforms that combine programmable logic, hard processors, and application-specific compute blocks within a single package.

2.2 FPGAs vs. DSPs and ASICs

The choice among FPGAs, DSP processors, and ASICs depends on the application's performance, flexibility, and cost requirements. DSP processors execute instructions sequentially and, while optimized for MAC-intensive operations, cannot match FPGAs for high-throughput, low-latency workloads requiring massive parallelism. FPGAs support true parallel execution of multiple operations and are well suited for high-throughput, low-latency tasks such as real-time SDR and multi-carrier modulation. DSPs, by contrast, are usually cheaper and benefit from software-centric

workflows that shorten development time, making them preferable when budgets or schedules are constrained.

ASICs deliver the highest performance per watt and are cost-effective at large production volumes, but their inflexibility restricts their applicability in scenarios involving rapidly changing communication standards. FPGAs occupy an intermediate position: they approach ASIC performance when correctly programmed, can be reconfigured post-deployment to correct bugs or introduce new features, and reach the market far faster than ASIC tape-outs. High-speed applications like SDR, satellite modems, and HDTV require very high performance not achievable with commonly available DSP processors, making FPGAs an attractive alternative despite their higher unit cost and design complexity relative to DSPs.

2.3 OFDM and Multi-Carrier Modulation on FPGAs

Orthogonal Frequency Division Multiplexing is a critical modulation technique for high-speed communication systems, particularly in the context of 5G networks. OFDM inherently performs its operations in a parallel fashion, making it vital that any implementation execute OFDM's processing pipeline in parallel by default. FPGAs offer significant advantages for implementing OFDM systems due to their flexibility, parallel processing capabilities, and efficiency. Recent review work published in IEEE conference proceedings synthesizes advances in FPGA-based OFDM implementations, covering FFT acceleration techniques, low-power designs, and phase compensation strategies as key design dimensions.

A particularly active research direction involves Orthogonal Time Frequency Space (OTFS) modulation for high-mobility scenarios envisioned for 6G systems. FPGAs are superior to traditional DSPs in wireless communication applications due to their high parallelism, flexibility, power efficiency, and speed. A complex modulation scheme like OFDM—or OTFS—requires real-time processing of large amounts of data; the high parallelism and low latency of FPGAs make them ideal for processing such signals. Several processing blocks are required, including the Fast Fourier Transform, Inverse FFT, modulation/demodulation, and channel estimation stages.

2.4 Error Correction Coding

Forward Error Correction (FEC) is an essential component of any reliable digital communication link. The wireless communication system relies on several coding schemes such as turbo codes, LDPC codes, convolutional codes, and polar codes. LDPC codes have emerged as the dominant choice for 5G NR data channels owing to their near-Shannon-limit performance and suitability for highly parallel hardware decoders. In 5G New Radio, LDPC decoding is performed using a belief propagation algorithm with layered decoding, where the code is divided into multiple layers decoded separately, enabling high throughput with moderate hardware resources.

Research articles comparing turbo and LDPC coding hardware architectures on Virtex-5 FPGAs show that turbo codes can achieve coding gain close to Shannon's limit, while LDPC codes provide robust error correction over noisy channels. A comprehensive review published in October 2023 evaluated LDPC decoder architectures across multiple FPGA implementations and concluded that FPGA platforms affirm their practicality and relevance in contemporary communication technology, offering comprehensive solutions to modern FEC requirements. The transition from turbo to LDPC and polar codes in 5G NR has driven renewed hardware implementation research targeting Xilinx UltraScale+ and Intel Agilex FPGA families.

2.5 MIMO and Massive MIMO

Multiple-Input Multiple-Output antenna systems multiply spectral efficiency by exploiting spatial degrees of freedom. MIMO-OFDM has been established as the key technology in modern wireless access standards. FPGA-based MIMO prototypes have demonstrated the practical feasibility of these systems: a real-time 4-stream MIMO-OFDM FPGA transceiver achieved a throughput of 216 Mbit/s over a 20 MHz bandwidth, covering all stages from RF to channel decoding. The prototype addressed algorithm and implementation aspects including initial parameter estimation, channel estimation, MIMO detection, parameter tracking, and channel decoding within a single FPGA platform.

Channel estimation is a key processing module in next-generation mobile wireless communications. Since the radio channel must be estimated for each combination of transmit and receive antennas in a MIMO system, the latency and cost-effectiveness of the implementation significantly influence overall system performance. Research on FPGA implementations of MIMO-OFDM channel estimation has demonstrated that resource-sharing through multiplexing techniques—where a single estimation module is time-shared among multiple antennas—can reduce hardware resource utilization by at least 43 percent while maintaining the same communication performance as baseline implementations.

2.6 Software-Defined Radio

Software-Defined Radio is a highly flexible communication system in which functions traditionally performed by analog hardware are instead implemented in software or configurable logic. SDR provides a reconfigurable architecture that enables multiple communication standards to coexist on generic hardware, allowing new wireless features and capabilities to be added to existing radio systems without hardware replacement. FPGAs typically operate in the 50–200 MHz clock range and, because of the parallel nature of digital hardware, can sustain very high throughput—permitting the transmission and reception of complex radio waveforms that general-purpose processors cannot handle at equivalent latency.

SDR technology was initially developed for military applications but is now widely used in analog and digital radio communication applications including WLAN, Bluetooth, GPS, WCDMA, and mobile communication. FPGA-based SDR transceivers replace multiple platform-based systems with a single reconfigurable platform, guaranteeing reliable, reconfigurable hardware implementations programmable via high-level languages. Despite these advantages, SDR platforms face challenges in power consumption and the limited speed of analog-to-digital and digital-to-analog converters for wideband, high-frequency applications.

3. Theoretical Framework

The analysis in this paper draws on four complementary frameworks. Shannon Information Theory provides the fundamental performance bounds—channel capacity, error exponent, and rate-distortion tradeoffs—against which hardware implementations of modulation and coding are evaluated. The concept of achievable rate under additive white Gaussian noise (AWGN) and fading channel models anchors the comparison of LDPC, turbo, and polar codes implemented on FPGA substrates.

Digital Hardware Design Theory, encompassing register-transfer level (RTL) modeling, pipelining, and parallelism, explains how FPGA logic resources are mapped to communication signal processing algorithms. Key principles include the use of pipelined FFT butterfly architectures for OFDM baseband processing, fixed-point arithmetic with careful word-length optimization to balance

computational accuracy and hardware cost, and resource sharing through time-multiplexing to minimize LUT and DSP slice consumption.

The Software Radio Architecture model, as formalized in the JTRS Software Communications Architecture and subsequent literature, defines the layered decomposition of a radio waveform into physically realizable modules: waveform components implemented in configurable hardware, middleware services managing resource allocation, and application-layer interfaces. This framework guides the partitioning of SDR functions between FPGA logic, embedded processor cores, and external RF front-ends in heterogeneous SoC platforms.

Systems Thinking is applied to analyze the interdependencies among FPGA device capability, algorithmic complexity, communication protocol requirements, and system-level performance metrics. Changes in one domain—for example, the increase in subcarrier count from LTE to 5G NR—propagate to FPGA resource requirements, FFT engine sizing, memory bandwidth, and timing closure. This holistic perspective enables a balanced assessment of FPGA viability across different communication application domains.

4. Methodology

This study employs a structured literature survey complemented by comparative performance analysis. Peer-reviewed publications from IEEE Xplore, ACM Digital Library, and Springer were surveyed for the period up to December 2024, with particular emphasis on contributions published between 2018 and 2024 to capture the most recent developments in FPGA toolchains, device families, and communication standards. Search terms included combinations of 'FPGA', 'digital communication', 'OFDM', 'MIMO', 'LDPC', '5G', 'SDR', 'reconfigurable hardware', and 'baseband processor'.

Inclusion criteria required that selected works (i) report quantitative hardware implementation results—such as resource utilization (LUTs, DSP slices, BRAMs), clock frequency, throughput, or power consumption—on identified FPGA devices; (ii) target a recognized communication standard or clearly defined communication algorithm; and (iii) provide sufficient implementation detail for comparative analysis. Works relying solely on floating-point software simulation without hardware synthesis results were excluded.

Comparative performance data were organized across three implementation categories—modulation and baseband processing, error correction coding, and transceiver prototyping—enabling cross-study comparison of resource efficiency and throughput normalized to device capacity. Where multiple studies targeted the same algorithm (e.g., LDPC decoding) on different device families, technology node differences were noted to contextualize comparisons. Limitations of this methodology include the heterogeneity of benchmark conditions across studies (differing modulation orders, code rates, device families, and synthesis tool versions) and the potential for publication bias toward high-performance results.

Table 1: Representative FPGA Implementation Results in Digital Communication Systems

Application	FPGA Device	Key Metric	Performance
OFDM Baseband (5G NR)	Xilinx UltraScale+	Throughput	>1 Gbps

4×4 MIMO-OFDM Transceiver	Xilinx Virtex-5	Data Rate	216 Mbps (20 MHz BW)
5G NR LDPC Decoder	Xilinx Virtex-7	Throughput	~1.5 Gbps
OTFS Modulator (6G Research)	Ettus USRP X410 (RFSoC)	BER (vs OFDM)	Superior in high-Doppler
SDR Transceiver (QPSK/QAM)	Intel Arria 10	Clock Frequency	200 MHz sustained
ANN-Based Equalizer	Xilinx UltraScale+	Throughput	~Gbps, exceeds GPU

5. Analysis And Discussion

5.1 FPGA as an Enabler for Physical Layer Implementation

The analysis confirms that FPGAs serve as a uniquely capable platform for implementing the physical layer of digital communication systems across a broad spectrum of applications. The combination of parallel hardware execution, deterministic timing, and post-deployment reconfigurability addresses requirements that neither DSP processors nor ASICs can simultaneously satisfy. Deterministic low-latency performance is a particularly significant advantage: FPGA designs operate at the hardware level without the variability of operating system scheduling or cache stalls, enabling audio and data communication paths to be fully pipelined and parallelized with sub-millisecond end-to-end latency—a characteristic critical for control plane signaling in 5G base stations and time-sensitive industrial wireless networks.

The integration of renewable processing efficiency is also noteworthy. Unlike ASICs, FPGA designs can be updated post-deployment, making it easier to introduce new codecs, filters, or protocols without hardware replacement. This capability has direct economic implications for network operators, who can update baseband firmware to support new 3GPP releases—such as the transition from 5G NR Release 15 to Release 17—without replacing installed radio units.

5.2 OFDM and FFT Implementation Considerations

OFDM implementation on FPGAs is dominated by the Fast Fourier Transform engine, which is the computationally most demanding block in terms of multiplier and memory resources. Pipelined FFT architectures using the radix-2 or radix-4 Cooley-Tukey algorithm are standard, and modern FPGAs provide dedicated FFT IP cores in their design tool ecosystems. For 5G NR, which requires IFFT/FFT sizes ranging from 128 to 4096 points depending on numerology and bandwidth, FPGA implementations must support variable transform sizes with minimal reconfiguration overhead. Research has shown that FFT acceleration techniques and phase compensation strategies are among the most active design considerations in recent FPGA-based OFDM implementations.

Low-power OFDM design is an emerging area, with researchers exploring approximate computing—trading marginal BER degradation for substantial reductions in dynamic power—on FPGAs deployed in battery-powered IoT edge nodes. Fixed-point word-length optimization is a pervasive challenge: insufficient mantissa bits introduce quantization noise that degrades the effective SNR of the OFDM

receiver, while excessive word lengths waste DSP slices and routing resources. Systematic fixed-point simulation followed by hardware synthesis remains the standard methodology for resolving this trade-off.

5.3 Error Correction Coding: LDPC and Turbo Implementations

LDPC decoding is a computationally intensive process that involves iteratively updating variable and check node messages according to the belief propagation algorithm. FPGA implementations must balance decoder throughput, BER performance, and logic resource consumption. The layered decoding technique adopted by 5G NR partitions the parity-check matrix into layers that can be decoded sequentially with pipelined message-passing, enabling high throughput with reduced resource requirements compared to flooding-schedule implementations. Published results for 5G NR LDPC decoders on Xilinx Virtex-7 class devices report throughputs of approximately 1–2 Gbps at operating frequencies of 200–250 MHz, meeting the physical layer requirements of sub-6 GHz 5G base station implementations.

Turbo codes, while largely superseded by LDPC in 5G NR data channels (polar codes are adopted for control channels), remain relevant in legacy LTE systems and satellite communications. Comparative hardware performance analysis shows turbo codes can achieve coding gain very close to Shannon's limit, whereas LDPC codes provide robust error correction with more parallelizable decoder architectures. The FPGA synthesis results consistently favor LDPC in terms of achievable throughput for equivalent logic resource budgets, which aligns with the 3GPP standardization decision for 5G NR.

5.4 MIMO and Channel Estimation

Massive MIMO—deploying 64 or more antenna elements at base stations to serve multiple user terminals simultaneously through spatial multiplexing and beamforming—represents one of the most computationally demanding signal processing workloads in 5G systems. FPGA-based prototyping platforms, particularly RFSoC devices that integrate analog front-end converters with programmable logic on a single die, have become the reference platform for massive MIMO research testbeds. The real-time matrix inversion and precoding computations required for zero-forcing or minimum mean-square error (MMSE) detectors in 64×8 MIMO configurations demand hundreds of GFLOPS, necessitating highly pipelined fixed-point matrix processor architectures within the FPGA fabric.

Channel estimation efficiency is directly linked to overhead and complexity. Pilot-based Least Squares estimation with cosine-domain noise suppression—implemented on FPGA with a proposed resource-sharing multiplexing technique—demonstrated savings of at least 43 percent of hardware resources while maintaining equivalent estimation accuracy to baseline approaches. Such optimizations are essential for scaling MIMO systems to higher antenna counts without proportionally increasing FPGA device costs, and they reflect a broader principle: algorithmic reformulation guided by hardware constraints yields implementations that outperform direct hardware mappings of textbook algorithms.

5.5 Software-Defined Radio and Cognitive Radio

FPGA-based SDR platforms such as the National Instruments USRP (Universal Software Radio Peripheral) series, which pair Xilinx Kintex or RFSoC FPGAs with wideband RF transceivers, have democratized radio research by providing reconfigurable hardware accessible to academic and industrial researchers alike. These platforms underpin experiments in cognitive radio, dynamic

spectrum access, and over-the-air testing of waveforms including LTE, 5G NR, and experimental OTFS waveforms for 6G research. The FPGA within such platforms handles time-critical baseband processing—synchronization, channel estimation, demodulation—while an embedded processor or host PC manages higher-layer protocol processing.

Cognitive radio, which builds on SDR by adding spectrum sensing and dynamic access capabilities, places additional demands on FPGA logic: the radio must sense occupied channels in near-real-time, make access decisions, and reconfigure its transmit waveform accordingly. Dynamic partial reconfiguration—a capability offered by modern Xilinx and Intel FPGA families—enables portions of the FPGA logic fabric to be reprogrammed while other portions remain operational, making it possible to switch waveform configurations without interrupting ongoing communication. This feature is particularly valuable for cognitive and multi-standard radio applications.

5.6 Challenges and Barriers

Despite their capabilities, FPGA-based communication systems face several persistent challenges. Design complexity is a primary barrier: implementing and verifying a complete communication physical layer in RTL requires expertise in both communication theory and digital hardware design, and development cycles are substantially longer than equivalent software implementations. High-Level Synthesis tools such as Xilinx Vitis HLS and Intel oneAPI partially mitigate this by allowing C/C++ or Python descriptions to be synthesized to RTL, but the performance gap between HLS-generated and hand-crafted RTL remains significant for throughput-critical functions.

Power consumption on the hardware board is a recognized challenge for FPGA-based SDR and communication systems. FPGA static power—dominated by leakage in the SRAM-based configuration memory—imposes a baseline power floor regardless of functional activity, making FPGAs less energy-efficient than ASICs at identical workloads in high-volume deployments. The speed of ADC and DAC components also becomes a limitation for wideband and high-frequency applications, with converter performance representing the practical bottleneck in many SDR system implementations. Additionally, many businesses and research groups—particularly smaller institutions and SMEs—lack the technical expertise to integrate FPGA designs into operational communication systems or to migrate existing software implementations to reconfigurable hardware substrates.

5.7 Role of Policy and Ecosystem

The FPGA ecosystem—comprising semiconductor vendors, IP core providers, EDA tool vendors, and research institutions—plays a critical role in the accessibility and advancement of FPGA-based communications. Vendor-supplied reference designs for LTE and 5G baseband processing lower the barrier for system integrators building on established foundations. Open-source FPGA communication platforms, including GNU Radio with FPGA back-ends, have further accelerated research adoption. Academic programs and industry training initiatives that develop expertise in HDL design and fixed-point arithmetic are essential for building the workforce capable of implementing and maintaining FPGA-based communication systems at scale.

6. Conclusion

This paper has provided a comprehensive examination of FPGA-based digital communication

systems, covering architectural fundamentals, key application domains, performance characteristics, and implementation challenges. FPGAs occupy an irreplaceable position in the digital communications landscape: their reconfigurability, parallel processing capability, and deterministic latency make them the platform of choice for prototyping advanced communication standards, deploying flexible SDR systems, and implementing computationally intensive physical layer functions such as massive MIMO processing and high-throughput LDPC decoding. The convergence of 5G deployment, the emergence of 6G research, and the proliferation of IoT and edge computing applications collectively ensure strong demand for FPGA-based communication hardware through the foreseeable future.

Nevertheless, significant challenges remain. Design complexity and the shortage of engineers proficient in both communication systems and digital hardware design limit the pace of adoption. Power efficiency relative to ASICs remains a disadvantage in high-volume commercial deployments. ADC and DAC speed constraints cap the achievable RF bandwidth of SDR platforms. Bridging these gaps will require advances in HLS tools and design automation, tighter integration between FPGA logic and RF analog front ends in RFSoC architectures, and broader engineering education initiatives.

Future research directions should prioritize the integration of machine learning inference within FPGA-based receivers for adaptive equalization and channel estimation under non-stationary channel conditions, as demonstrated by emerging neural network transceiver designs achieving Gbps throughput with FPGA acceleration. Additionally, the development of FPGA implementations for OTFS modulation targeting 6G high-mobility scenarios represents an important open area, as current results remain largely confined to simulation. Regional heterogeneity in FPGA adoption—driven by differences in semiconductor supply chains, spectrum regulation, and educational infrastructure—should also be examined to support equitable global development of advanced communication systems.

7. References

1. IEEE Transactions on Reconfigurable Technology and Systems. (2023). Introduction to the Special Section on FPGA 2023. ACM Transactions on Reconfigurable Technology and Systems, 16(4). doi:10.1145/3695841
2. Ozan, W., et al. (2023). FPGA Implementation of OTFS Modulation for 6G Communication Systems. arXiv preprint arXiv:2310.09671.
3. IEEE Xplore. (2024). FPGA-based OFDM Systems for 5G and High-Speed Communication: A Comprehensive Review. IEEE Conference Publication. doi:10.1109/10800844
4. IEEE Xplore. (2012). FPGA Implementation of Modern Wireless Communication System. IEEE Conference Publication. doi:10.1109/6335374
5. Fekry, S., Zekry, A. H. A., Hassan, A. Y., & Shiple, M. M. (2023). FPGA Implementation of 5G NR LDPC Codes. Advances in Science, Technology and Engineering Systems Journal, 8(4).
6. Delomier, Y., Le Gal, B., Crenne, J., & Jego, C. (2020). Model-Based Design of Flexible and Efficient LDPC Decoders on FPGA Devices. Journal of Signal Processing Systems, 92(7), 749–762.
7. IIETA. (2023). A Comprehensive Review and Evaluation of LDPC Implementations. International Information and Engineering Technology Association, 28(5), 1113–1125.
8. Rashmi, R., & Devi, M. (2022). FPGA Performance Analysis of LDPC and Turbo Codes for Communication System. ResearchGate.
9. Ramesh, S., & Seshasayanan, R. (2016). FPGA implemented testbed in 8-by-8 and 2-by-2 OFDM–MIMO channel estimation and design of baseband transceiver. SpringerPlus, 5(1), 1–

15. doi:10.1186/s40064-016-1827-z
10. IEEE Xplore. (2018). Efficient Implementation of DCT-based MIMO Channel Estimation on FPGA. IEEE Conference Publication. doi:10.1109/8471834
11. IEEE Xplore. (2011). FPGA implementation of channel estimation for MIMO-OFDM. IEEE Conference Publication. doi:10.1109/5937663
12. Gesbert, D., et al. (2008). A real-time 4-stream MIMO-OFDM transceiver: System design, FPGA implementation, and characterization. IEEE Transactions on Signal Processing, 56(7).
13. UTC Scholar. (n.d.). An Evaluation of Low Cost FPGA-Based Software Defined Radios. University of Tennessee at Chattanooga.
14. Ahmad, A. I., & Erkal, B. (2022). FPGA based implementation of SDR transceiver. European Journal of Science and Technology (EJOSAT).
15. IEEE Xplore. (2014). FPGAs in Software Defined Radio. IEEE Conference Publication. doi:10.1109/6710521
16. IntechOpen. (2017). FPGA-Based Software-Defined Radio and Its Real-Time Implementation Using NI-USRP. IntechOpen Chapters.
17. Ampheo. (2024). What are the differences between FPGA and DSP processors for signal processing? Ampheo Technical Blog. Retrieved from https://www.ampheo.com
18. Logic Fruit Technologies. (2023). Digital Signal Processing with FPGAs for Accelerated AI. Logic Fruit Blog. Retrieved from https://www.logic-fruit.com
19. Patsnap Eureka. (2023). FPGA vs ASIC: Which is better for digital signal processing? Patsnap Technical Articles.
20. Meyer-Baese, U. (2007). Digital Signal Processing with Field Programmable Gate Arrays (3rd ed.). Signals and Communication Technology. Springer.