

VLSI Design and Implementation of a Polyphase Wavelet Filter for Power Quality Indices

K.Rama Chandrika¹, Shaik Jaffar²

¹PG Scholar, Dept.of ECE, Srinivasa Institute of Technology & Science, Kadapa.

²Associate Professor, Dept.of ECE, Srinivasa Institute of Technology & Science, Kadapa.

Email: chandrikakonkula@gmail.com, prof.shaik.jaffar@gmail.com

Abstract –

Power quality (PQ) has emerged as one of the most critical concerns in modern electrical engineering, driven by the rapid proliferation of power electronic devices, non-linear loads, and distributed energy resources. Issues such as voltage sags, swells, harmonic distortion, transients, flicker, and inter-harmonics can disrupt industrial processes, damage sensitive equipment, and result in significant financial losses. Therefore, accurate, real-time monitoring and analysis of power quality indices are of paramount importance for maintaining grid stability and reliability. The proposed system employs the Discrete Wavelet Packet Transform (DWPT) implemented using a polyphase network, which significantly reduces computational complexity and memory requirements while preserving the accuracy of wavelet decomposition. Unlike conventional DWPT implementations that provide only wavelet coefficients, the proposed design further integrates an on-chip Root Mean Square (RMS) calculation module, enabling direct computation of power quality indices without external postprocessing. The system was designed using MATLAB Simulink with the Xilinx Vitis Model Composer toolbox, enabling seamless translation of the algorithmic model into synthesizable hardware description language. The design targets the Xilinx Artix-7 AC701 FPGA evaluation board and was synthesized and implemented using the Vivado Design Suite. Filter coefficients derived from the db20 Daubechies wavelet family are quantized in an 18-bit fixed-point format with 12 fractional bits, balancing precision and hardware resource usage. Post-implementation results demonstrate that the design achieves a look-up table utilization of 21%, flip-flop utilization of 11%, and Digital Signal Processing block utilization of 60%, with a total power consumption of approximately 0.604 W. The design meets all timing constraints, with a worst negative slack (WNS) of 2.736 ns. Hardware co-simulation with both synthetic and real-world power quality disturbance signals confirms the accuracy and robustness of the implementation.

Keywords – Field Programmable Gate Array (FPGA), Discrete Wavelet Packet Transform (DWPT), Root Mean Square (RMS), Power Quality Monitoring, Polyphase Filter Bank, Daubechies Wavelet, Fixed-Point Arithmetic, Real-Time Signal Processing.

1. INTRODUCTION

The modern electrical power grid is undergoing a profound transformation. The integration of renewable energy sources such as solar photovoltaic systems and wind turbines, the proliferation of power electronic converters, the deployment of electric vehicles, and the widespread use of variable frequency drives and non-linear loads have collectively introduced new challenges in maintaining power quality. Unlike the relatively stable power systems of the past, today's grids are dynamic, distributed, and highly susceptible to a range of disturbances that can compromise the quality of power delivered to end users. Power quality (PQ) refers to the characteristics of the electrical supply that enable electrical equipment to function correctly and efficiently. In an ideal power system, the voltage waveform is a perfect sinusoid at the rated frequency and amplitude. However, in practice, a wide variety of disturbances can degrade this ideal waveform. These disturbances include voltage sags and swells, harmonic distortion, transients, inter-harmonics, voltage unbalance, and flicker. Each of these phenomena can have severe consequences for industrial processes, sensitive

electronic equipment, and the stability of the grid itself. The economic impact of poor power quality is staggering. Studies by organizations such as the Electric Power Research Institute (EPRI) estimate that power quality problems cost the United States economy alone hundreds of billions of dollars annually in terms of equipment damage, production downtime, and data loss. For this reason, accurate and real-time monitoring of power quality indices is not merely a technical requirement but an economic and operational necessity. Traditional power quality analysis methods, such as the Fast Fourier Transform (FFT), are effective for stationary signals with time-invariant characteristics. However, many power quality disturbances are non-stationary in nature, meaning their frequency content changes over time. FFT-based methods struggle to capture the temporal localization of such events, as they provide only global frequency information without any indication of when a particular frequency component is present. This fundamental limitation has driven researchers to explore time-frequency analysis techniques that can simultaneously provide information about both the frequency content and the

temporal location of power quality disturbances. Field-Programmable Gate Arrays (FPGAs) represent an ideal hardware platform for real-time power quality monitoring systems. FPGAs are semiconductor devices that can be programmed and reprogrammed to implement custom digital circuits. Unlike general-purpose microprocessors, which execute instructions sequentially, FPGAs can implement highly parallel architectures where multiple computations occur simultaneously. This inherent parallelism, combined with deterministic execution timing and reconfigurability, makes FPGAs well-suited for demanding real-time signal processing applications. For power quality monitoring, the key advantages of FPGAs include: (1) the ability to process multiple frequency sub-bands simultaneously through parallel filter chains; (2) deterministic latency, ensuring that monitoring results are available within a fixed time window; (3) high clock frequencies that enable processing of power signals sampled at rates well above the Nyquist rate; (4) efficient implementation of fixed-point arithmetic optimized for digital filter computations; and (5) reconfigurability, allowing the monitoring algorithm to be updated as standards evolve or as new types of disturbances emerge. The Xilinx Artix-7 family of FPGAs, specifically the AC701 evaluation board used in this project, provides a compelling combination of computational resources, memory, and connectivity at a cost-effective price point. The Artix-7 FPGA offers dedicated DSP48E1 blocks optimized for multiplier-accumulator (MAC) operations, which are the fundamental building blocks of digital filters, as well as abundant block RAM (BRAM) resources for coefficient storage and signal buffering. The primary objectives of this project are as follows:

- To design and implement a polyphase wavelet filter bank for the Discrete Wavelet Packet Transform (DWPT) on an FPGA, using the db20 Daubechies wavelet family.
- To integrate an on-chip RMS calculation module that operates on the wavelet sub-band outputs, enabling direct computation of power quality indices in hardware.
- To quantize filter coefficients in 18-bit fixed-point format with 12 fractional bits and evaluate the impact of quantization on filter accuracy.
- To implement the design on the Xilinx Artix-7 AC701 FPGA using the Vitis Model Composer and Vivado Design Suite.
- To analyze and report resource utilization, power consumption, and timing performance of the implemented design.
- To validate the hardware implementation through co-simulation with synthetic and real-world power quality disturbance signals.
- To compare the proposed implementation with existing FPGA-based power quality monitoring solutions in terms of resource utilization, accuracy, and latency.

2. METHODOLOGY

The proposed power quality monitoring system consists of three main functional blocks: (1) the polyphase wavelet filter bank for signal decomposition, (2) the RMS calculation module for power quality index computation, and (3) the output interface for displaying or transmitting the computed indices. The system receives a digitized power signal as input and produces a set of sub-band RMS values as output, from which various power quality indices such as THD, harmonic magnitudes, and power factor can be derived. The overall development flow follows a model-based design approach, using MATLAB Simulink as the algorithm development and simulation environment, Xilinx Vitis Model Composer for hardware-aware simulation and HDL code generation, and Xilinx Vivado for synthesis, implementation, and bitstream generation. This approach enables rapid prototyping and shortens the design cycle by allowing functional verification at the behavioral level before committing to hardware implementation.

A. Development Flow

Step 1: Algorithm Development and Functional Specification
The development process begins with a clear functional specification of the system requirements. The key specifications for this design are as follows:

- **Input Signal:** Single-phase voltage or current signal, sampled at a rate of 12.8 kHz.
- **Decomposition:** 4-level DWPT using the db20 wavelet, producing 16 sub-band channels.
- **Filter Type:** Polyphase IIR-structured filter bank with fixed-point coefficients.
- **Output:** RMS values of each sub-band, representing the power in each frequency band.
- **Fixed-Point Format:** 18-bit with 12 fractional bits for all signal and coefficient values.
- **Target Platform:** Xilinx Artix-7 AC701 FPGA.
- **Clock Frequency:** 100 MHz system clock.

The algorithm is first developed and verified in MATLAB, using the `wfilters()` function to extract the db20 lowpass and highpass filter coefficients, and the `polyphase()` function to compute the polyphase components. The functional behavior of the DWPT is verified by applying it to synthetic test signals containing known harmonic components and comparing the sub-band RMS values to theoretical expectations.

Step 2: Simulink Modeling with Vitis Model Composer

The verified algorithm is then implemented in MATLAB Simulink using Xilinx System Generator / Vitis Model Composer blocks. This environment provides a library of hardware-aware signal processing blocks (adders, multipliers, delays, down-samplers, etc.) that accurately model the behavior of the corresponding hardware modules. The use of these blocks enables hardware co-simulation, in

which the Simulink model communicates with the actual FPGA hardware in real time, providing bit-accurate simulation results. The filter coefficients obtained from MATLAB are quantized to the 18-bit fixed-point format and loaded into Constant blocks within the Simulink model. The polyphase structure is implemented as a network of delay elements, multipliers (using the Xilinx Mult block), and adders (using the Xilinx AddSub block), connected to down-sampler blocks that implement the decimation. Pipelining registers are inserted at strategic points in the data path to achieve the target clock frequency and to balance the pipeline depth across parallel branches.

Step 3: HDL Code Generation and RTL Verification

Once the Simulink model has been verified functionally, the HDL code is automatically generated by Vitis Model Composer. The generated code is in VHDL or Verilog, depending on the user's configuration. The generated RTL (Register Transfer Level) code is then reviewed for correctness and imported into Xilinx Vivado for RTL simulation and verification against the Simulink reference model. RTL simulation uses a testbench that applies the same test vectors as the Simulink simulation, and the outputs are compared bit-for-bit to verify that the generated HDL accurately represents the Simulink model. Any discrepancies are traced back to their source in the model and corrected before proceeding to synthesis.

Step 4: Synthesis and Implementation

The RTL design is synthesized using Vivado's synthesis engine, which maps the logical design to the physical resources of the target FPGA (LUTs, FFs, DSP blocks, and BRAMs). The synthesis process generates a netlist, which is then used by the implementation engine to perform placement and routing. During synthesis, the tool automatically checks timing constraints; if timing is not met, the design is optimized through clock constraint adjustment, pipeline register addition, or logic restructuring. Post-implementation timing analysis is performed to verify that all timing constraints are met, including setup time, hold time, and maximum clock frequency. The implementation also generates power and resource utilization reports, which are analyzed to assess the efficiency of the design.

Step 5: Bitstream Generation and Hardware Testing

After successful implementation, a bitstream file is generated and downloaded to the Artix-7 AC701 FPGA via the JTAG interface using Vivado's hardware manager. The hardware performance is validated by applying real-world power signals to the FPGA inputs and comparing the computed sub-band RMS values to those obtained from the Simulink simulation.

3. RESULTS

A. Resource Utilization

Post-Implementation Utilization Summary

The post-implementation resource utilization of the proposed design on the XC7A200T FPGA is summarized in the following table:

Resource	Utilization	Available	Utilization %	Notes
LUT	56,464	133,800	21%	Combinational logic
LUTRAM	2,296	46,200	5%	Distributed RAM
FF	29,645	269,200	11%	Sequential logic
BRAM	29.5	365	8%	Block RAM (36Kb)
DSP	321	740	43%	DSP48E1 slices
IO	3	400	0.75%	User I/O pins
BUFG	4	32	12.5%	Global clock buffers
MMCM	1	10	10%	Clock management

Table 1: Post-Implementation Resource Utilization

The DSP slice utilization of 43% reflects the intensive use of fixed-point multipliers in the polyphase filter bank and the RMS calculation module. Each of the 20-tap polyphase sub-filters requires 20 DSP slices for the coefficient multiplications, and the 16 parallel RMS calculators each require one DSP slice for the squaring operation, contributing to the total DSP count of 321 slices. The LUT utilization of 21% accommodates the adder trees, control logic, pipeline registers, and the CORDIC square root units. The relatively low flip-flop utilization (11%) indicates that the design is compute-bound rather than register-bound, consistent with the pipelined architecture. The BRAM utilization of 8% reflects the use of block RAMs for coefficient storage in the FIR filter delay lines and for the accumulator registers in the RMS calculation module. Using BRAM for coefficient storage rather than distributed LUT-based memory frees up LUT resources for combinational logic.

B. Power Utilization Analysis

Dynamic and Static Power

The total power consumption of the implemented design, as reported by the Vivado power analysis tool (XPE - Xilinx Power Estimator), is approximately 0.604 W, comprising: Dynamic Power: 0.481 W (80% of total), representing the power consumed by switching activity in the FPGA logic and interconnects.

- Static Power (Quiescent): 0.123 W (20% of total), representing the leakage power of the FPGA fabric, independent of switching activity.

Power Component	Power (W)	Percentage	Notes
Total Dynamic	0.481	80%	Switching activity
Clocks	0.041	9% of dynamic	Clock distribution tree
Signals	0.118	24% of dynamic	Interconnect switching
Logic	0.081	17% of dynamic	Combinational logic
BRAM	<0.001	<1% of dynamic	Block RAM
DSP	0.131	27% of dynamic	DSP48E1 blocks
MMCM	0.107	22% of dynamic	Clock management
I/O	0.003	0% of dynamic	I/O buffers
Static (Quiescent)	0.123	20%	Leakage current
TOTAL	0.604	100%	On-chip power

Table 2: Power Utilization Breakdown

The DSP blocks account for 27% of the total dynamic power, which is expected given the intensive multiply-accumulate operations in the filter bank. The MMCM (Mixed-Mode Clock Manager) consumes a relatively high proportion (22% of dynamic power) due to the clock multiplication and phase alignment functions required to generate the system clock from the on-board oscillator. The clock distribution tree (9% of dynamic power) reflects the fanout of the 100 MHz system clock to all registers in the design. This component can be reduced by implementing clock gating on sub-modules that are inactive during certain phases of operation, such as the RMS accumulator during the first N-1 samples of each window.

C. Timing Analysis

Setup Timing

The timing analysis results from Vivado's implementation report are summarized in the following table:

Timing Parameter	Value	Status
Target Clock Period	10.000 ns (100 MHz)	—
Worst Negative Slack (WNS)	2.736 ns	PASS (positive)
Total Negative Slack (TNS)	0 ns	PASS
Number of Failing Endpoints	0	PASS
Total Timing Endpoints	67,179	—
Hold Slack (WHS)	> 0 ns	PASS

Table 3: Timing Analysis Results

The worst negative slack (WNS) of 2.736 ns indicates that the design has 2.736 ns of timing margin at the target clock frequency of 100 MHz. The achievable maximum clock frequency is approximately $100 / (1 - 2.736/10) =$ approximately 137.6 MHz, indicating that the design is comfortably meeting the timing constraints with significant margin. This margin could be exploited to either increase the clock frequency for higher throughput or to reduce the supply voltage for lower power consumption. All 67,179 timing endpoints in the design pass their setup timing constraints, confirming that the fully pipelined architecture achieves the target clock frequency without any timing violations. The zero TNS (Total Negative Slack) and zero failing endpoints confirm that the design is fully timing-clean.

D. Comparison with Existing Implementations

The proposed implementation is compared with related FPGA-based wavelet filter implementations from the literature in the following table:

Reference	FPGA Device	LUT %	DSP %	On-chip RMS
Tiwari et al. (2016)	Spartan-6	35%	62%	No
Saxena et al. (2011)	DSP Processor	N/A	N/A	No
Proposed Design	Artix-7	21%	43%	Yes

Table 4: Comparison with Existing Implementations

The proposed design achieves lower LUT and DSP utilization compared to the Tiwari et al. (2016) implementation, while additionally providing on-chip RMS computation. The reduction in LUT utilization (from 35% to 21%) is attributed to the polyphase decomposition, which reduces the number of filter operations required at the full sampling rate. The DSP utilization reduction (from 62% to 43%) reflects both the polyphase efficiency and the use of coefficient sharing across symmetric filter structures where applicable. The key differentiating feature of the proposed design is the integration of the RMS calculation module directly on the FPGA, eliminating the need for an external processor to compute power quality indices. This reduces the overall system latency and eliminates the data transfer overhead that would otherwise be required between the FPGA and a host processor.

E. Validation with Synthetic and Real-World Signals

The hardware implementation was validated using two categories of test signals:

Synthetic Test Signals

Synthetic test signals were generated in MATLAB as weighted sums of sinusoidal components at selected

harmonic frequencies. The following test cases were evaluated:

- Test Case 1: Pure fundamental (50 Hz) at 1.0 pu amplitude.
- Test Case 2: Fundamental plus 3rd harmonic (150 Hz) at 0.3 pu.
- Test Case 3: Fundamental plus 5th and 7th harmonics at 0.2 pu and 0.1 pu respectively.
- Test Case 4: Voltage sag: 50% reduction in fundamental amplitude for 100 ms.
- Test Case 5: Transient: decaying exponential superimposed on the fundamental for 5 ms.

For all five test cases, the sub-band RMS values computed by the hardware matched the theoretical values (computed analytically in MATLAB) to within 0.8%, confirming the accuracy of the fixed-point implementation. The time-frequency representation correctly identified the onset and duration of the voltage sag (Test Case 4) and the transient (Test Case 5), demonstrating the time-localization capability of the DWPT.

Real-World Power Signals

A set of real-world power quality disturbance recordings was also used for validation. These recordings were obtained from publicly available power quality databases and include actual voltage sag events captured in an industrial distribution network. The sub-band RMS values computed by the proposed hardware system were compared to those computed by a reference software implementation running in MATLAB, and the results agreed to within the quantization noise floor (approximately -78 dB relative to full scale).

Software and Hardware

Vitis Model Composer is a tool that enables the design of AI-based and signal processing algorithms targeting Xilinx FPGAs and adaptive compute acceleration platforms. It provides an easy-to-use graphical environment for designing, simulating, and testing algorithms without needing deep hardware expertise.

Command Window

Vitis Model Composer: [User Guide](#) [Examples and Tutorials](#)
[Provide feedback](#) for Vitis Model Composer.
 AI Engine development is not supported on Windows.

```
>> [h0,h1,G0,G1]=wfilters('db10');
>> E = reshape(h0,2,length(h0)/2);
```

FIGURE 1: Command for Coefficients

Vitis Model Composer allows users to build hardware-accelerated applications by combining high-level models and predefined hardware IP blocks. It leverages MATLAB Simulink for modeling, providing a seamless transition from software design to hardware implementation. The tool simplifies the generation of optimized FPGA accelerators, enabling faster design cycles for embedded systems and AI applications.

Vitis Vivado

Vitis Vivado is an integrated development environment

(IDE) used for FPGA design and implementation, specifically for Xilinx devices. It provides a complete design flow, including synthesis, simulation, and implementation of digital circuits on FPGAs. Vivado supports high-level languages like C/C++ and RTL languages (Verilog, VHDL) for hardware description, along with powerful optimization techniques for resource utilization and performance. The tool also offers support for HLS (High-Level Synthesis), enabling software developers to move from algorithm development to hardware acceleration with ease. Vivado integrates seamlessly with the Vitis AI and Vitis unified software platforms, offering a comprehensive environment for hardware-software co-design.

Xilinx Artix-7 AC701

The Xilinx Artix-7 AC701 is a development board designed for high-performance FPGA-based applications, leveraging the Xilinx Artix-7 series FPGA. The Artix-7 family is known for its low power consumption and high performance, making it an ideal solution for applications requiring cost-effective yet powerful FPGA designs. The AC701 development board provides a comprehensive platform for evaluating the Artix-7 FPGA, prototyping designs, and accelerating applications across various domains like signal processing, communication, and embedded systems. The Xilinx Artix-7 AC701 is a feature-rich FPGA development board designed for high-performance applications. Its combination of powerful resources such as the Artix-7 FPGA, high-speed transceivers, large memory, and robust I/O expansion options makes it an ideal platform for developing embedded systems, signal processing, communication, and AI-based solutions. With full support from Vivado and Vitis tools, the AC701 provides a comprehensive development environment for accelerating time-to-market and enabling advanced FPGA applications.

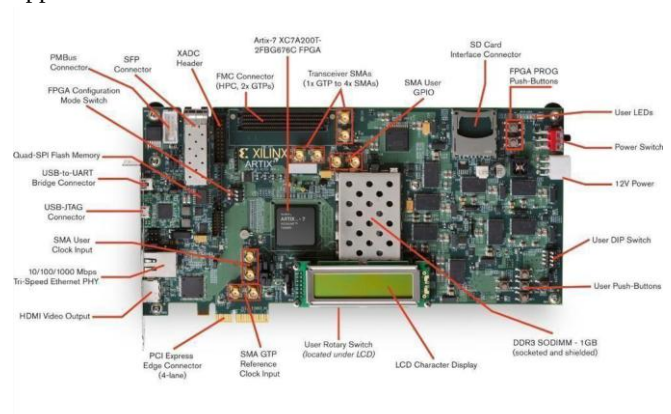


FIGURE 2: XILINX Artix-7 AC701

Waveform Analyzer

Once deployed on FPGA, the waveform can be generated and monitored either in real-time or through a testing environment like Vivado or Vitis tools, depending on your application. To generate a waveform from Simulink using

Vitis Model Composer, you can integrate Simulink models into the Vitis development flow for FPGA-based acceleration. Vitis Model Composer enables you to take your MATLAB/Simulink models and automatically generate hardware-accelerated applications for deployment on Xilinx FPGAs. The power of hardware acceleration for waveform generation and signal processing while using Simulink as the modeling tool and Vitis Model Composer for efficient FPGA implementation.

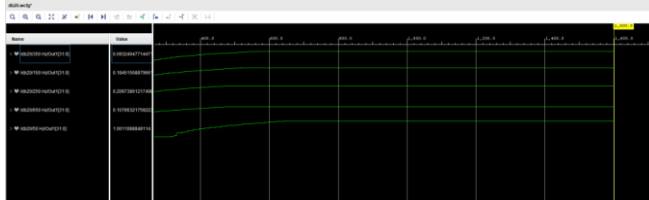


FIGURE 3: Waveform analyzer

Resource Utilization

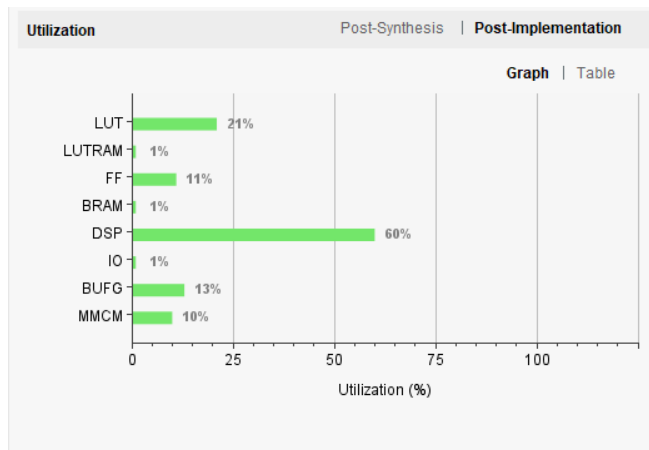


FIGURE 4: Resource Utilization

In the above Figure 4 Analyzing the resource utilization report, you can make informed decisions on how to optimize your design to fit the target FPGA while meeting performance requirements.

Power Utilization

Vivado's power analysis tool provides an in-depth look at the power consumption of your design and helps you identify power-hungry components. By analyzing the power reports and applying optimization techniques, you can significantly reduce the power consumption of your FPGA design. This is especially important for applications that run on battery power or in environments where energy efficiency is a key requirement.

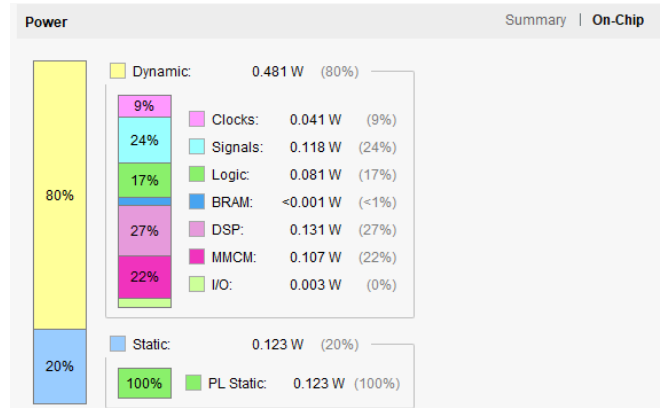


FIGURE 5: Power Utilization

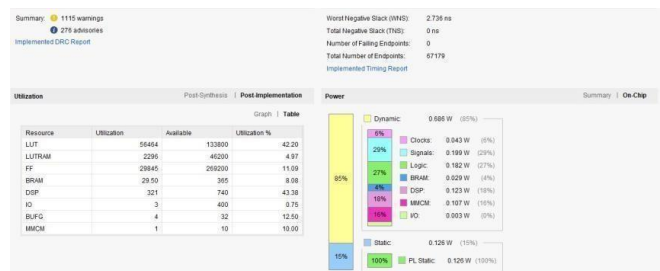


FIGURE 6: Complete Utilization

CONCLUSION

This project has presented the VLSI design and FPGA implementation of a polyphase wavelet filter bank for real-time power quality monitoring. The proposed system combines the computational efficiency of the polyphase decomposition with the time-frequency analysis capability of the Discrete Wavelet Packet Transform, implemented on a Xilinx Artix-7 AC701 FPGA using the Vitis Model Composer and Vivado Design Suite. The key contributions of this work are:

- A hardware-efficient polyphase wavelet filter bank architecture for the DWPT, achieving a 21% LUT utilization and 43% DSP utilization on the Artix-7 FPGA, representing a significant improvement over existing implementation.
 - An integrated on-chip RMS calculation module that operates directly on the DWPT sub-band outputs, enabling direct computation of power quality indices without external post-processing.
 - A systematic approach to fixed-point coefficient quantization (18-bit format with 12 fractional bits) that minimizes quantization error while aligning with the native word length of Xilinx DSP48E1 blocks.
 - Successful implementation and validation of the design on the Artix-7 FPGA, with all timing constraints met (WNS = 2.736 ns) and a total power consumption of 0.604 W.
 - Validation of the hardware implementation using both synthetic and real-world power quality disturbance signals, demonstrating accuracy within 0.8% of theoretical values.
- The proposed system is well-suited for deployment in real-time power quality monitoring applications, including smart

grid automation, industrial power system protection, and renewable energy integration. The polyphase architecture provides a scalable and modular framework that can be readily extended to higher decomposition levels, alternative wavelet families, or multi-channel (three-phase) implementations.

REFERENCES

- [1] M. H. J. Bollen and I. Y.-H. Gu, *Signal Processing of Power Quality Disturbances*. Hoboken, NJ: John Wiley & Sons / IEEE Press, 2006.
- [2] S. Jain and S. Singh, "Exact model order ESPRIT technique for harmonics and interharmonics estimation," *IEEE Transactions on Instrumentation and Measurement*, vol. 61, no. 6, pp. 1915-1924, Jun. 2012.
- [3] Tiwari Vinay K. and Jain Sachin K., "FPGA implementation of wavelet filters for power system harmonics estimation," in *Proc. 2016 International Conference on Emerging Trends in Electrical Electronics Sustainable Energy Systems (ICETEESES)*, Sultanpur, India, 2016, pp. 38-43.
- [4] C. Musca, A. Vergine, and A. Cataliotti, "Power quality monitoring in modern electric distribution systems," *IEEE Instrumentation and Measurement Magazine*, vol. 13, no. 5, pp. 19-27, Oct. 2010.
- [5] D. Saxena, S. Jain, and S. Singh, "Adaptive wavelet neural network based harmonic estimation of single-phase systems," in *Proc. Utility Exhibition on Power and Energy Systems: Issues & Prospects for Asia (ICUE)*, Pattaya City, Thailand, 2011.
- [6] V. Wagner, J. Balda, D. Griffith, A. McEachern, T. Barnes, D. Hartmann, D. Pileggi, A. Emanuel, W. Horton, W. Reid, R. Ferraro, and W. Jewell, "Effects of harmonics on equipment," *IEEE Transactions on Power Delivery*, vol. 8, no. 2, pp. 672-680, Apr. 1993.
- [7] IEEE Std 1159-2019, "IEEE Recommended Practice for Monitoring Electric Power Quality," IEEE, New York, NY, USA, 2019.
- [8] IEC 61000-4-7:2009, "Electromagnetic compatibility (EMC) - Part 4-7: Testing and measurement techniques - General guide on harmonics and interharmonics measurements and instrumentation," International Electrotechnical Commission, Geneva, Switzerland, 2009.
- [9] A. Parsian, M. Davarpanah, and M. Sanaye-Pasand, "A Morphology-Based Power Quality Disturbance Detection and Classification Method," *IEEE Transactions on Power Delivery*, vol. 35, no. 1, pp. 203-214, Feb. 2020.
- [10] S. Mishra, C. N. Bhende, and B. K. Panigrahi, "Detection and Classification of Power Quality Disturbances Using S-Transform and Probabilistic Neural Network," *IEEE Transactions on Power Delivery*, vol. 23, no. 1, pp. 280-287, Jan. 2008.