ISSN 2319-5991 www.ijerst.com

Peer Reviewed, Referred & Indexed Journal

Research Paper

A CHARGE EQUALIZED DYNAMIC COMPARATOR FOR LOW-POWER SUCCESSIVE APPROXIMATION ADC

[1] Marella Anush Raj, [2] Dr.K.Venkatachalam, [3] Venkata Sunil Srikanth

[1]M.Tech Scholar, Dept of ECE, Audisankara College of Engineering and Technology, Gudur, Andhra Pradesh

[2] Asssociate Professor, Dept of ECE, Audisankara College of Engineering and Technology, Gudur, Andhra Pradesh.

[3] Assistant Professor, Dept of ECE, Audisankara College of Engineering and Technology, Gudur, Andhra Pradesh

[1]anush.raj98@gmail.com [2]venkatmek12@gmail.com [3]sunilsrikanthv.ece@audisankara.ac.in

ABSTRACT: This paper provides a critical review and the classification of comparators in low-power lowdata-rate (1 kS/s~1.5 MS/s) successive approximation register analog-to-digital converters (SAR ADCs). Both voltage-domain and time-domain comparators are studied and their pros and cons are examined. The architecture, comparison time, and power consumption of five widely used voltage-domain dynamic comparators are studied first. It is followed with an investigation of kickback in comparators. We show although clock kickback is common-mode, the impedance asymmetry of the digital-to-analog converters (DACs) of SAR ADCs arising from the different resistances of DAC switches gives rise to a differential clock kickback that occurs earlier than output kickback with more strength hence dictating kickback in dynamic comparators. If the strength and duration of clock kickback are sufficiently large, the comparator will yield an erroneous output. The dependence of clock kickback on the input of SAR ADCs in the least significant bit (LSB) conversion is also investigated. The offset voltage of the dynamic comparators and its dependence on supply voltage are investigated, and the minimum tuning bits of digitally tuned offset compensation capacitor arrays is obtained. The noise of dynamic comparators is also investigated and design trade-offs between noise, power consumption, kickback, and the loading of the comparator on DAC are examined. The extensive simulation results of the comparators designed in a TSMC 130 nm 1.2 V CMOS technologies with reduced supply voltages and analyzed using Spectre from Cadence Design Systems with BSIM 3.3 device models are provided.

INDEX TERMS: Successive approximation register analog-to-digital converter, voltage-domain comparator, and time-domain comparator.

I. INTRODUCTION

Although the distinct characteristics of successive approximation register analog-to-digital converters (SAR ADCs) including low power consumption and good technology compatibility make them ideal candidates for power-constrained applications [1], [2], [3],

[4], the power consumption of these ADCs rises exponentially with resolution, as observed in Fig. 1. The power consumption of a SAR ADC is dictated by the power consumption of its digital-toanalog converter (DAC), comparator, and SAR. The power consumption of the DAC can be minimized using top-plate sampling where the most significant bit (MSB) is determined by comparing the inputs of the comparator directly without capacitor switching [5], [6], [7], staged capacitor array DACs where a set of bridged small binary-weighted capacitor arrays jointly function as a large binary-weighted capacitor array without large capacitors [8], [9], [10], and energy-efficient capacitor-switching schemes such as monotonic capacitor switching where only one capacitor down-switching per bit conversion is needed [11], [12], [13], input-range adaptive capacitor switching [14], and by-pass window capacitor switching [15], to name a few. The power consumption of voltage-domain comparators rises rapidly with resolution due to the need for large input transistors to minimize both the noise and offset voltage of the comparators and a pair of digitally tuned capacitor arrays for offset voltage compensation. The power consumption of time-domain comparators also rises sharply with resolution because the voltages to be compared need to propagate through a large number voltage-controlled delay stages in order to generate a large time variable whose polarity can be determined using an arbiter without difficulty. As the power consumption of the comparator constitutes approximately 30% of the overall power consumption of SAR ADC, as evidenced in Table 1, reducing the power consumption of the comparator without sacrificing resolution is pivotal in minimization of the overall power consumption of SAR ADC. To reduce the power consumption of comparators while continuing to improve resolution, various architectures of voltage-domain comparators emerged. These architectures include static comparators [16], [17], semidynamic comparators [18], [19], fully dynamic comparators with an explicitly clocked latch [6], [20], [21], [22], [23], [24], [25], [26] or an implicitly clocked latch [27], [28], [29], [30], [31]. Time-domain comparators to combat the difficulties encountered in design of low-power highresolution voltage-domain comparators also emerged. These comparators include voltage-controlled delay line (VCDL) comparators [8], [9], [32], [33], voltage-controlled oscillator (VCO) comparators [34], [35], [36], and edge-pursuit comparators [37], [38]. An in-depth examination of the pros and cons of these comparators, though critical to the design of low-power SAR ADC, however, is absent.

II. LITERATURE REVIEW:

80-MHz 8-bit CMOS Folding ADC
A high-speed 8-bit folding ADC using 0.5 µm CMOS technology is presented with distributed track-and-hold preprocessing. It operates at 80 MHz while consuming 80 mW from a 3.3 V supply. The architecture improves input frequency handling and reduces track-and-hold amplifier requirements.

10b/12b 40 kS/s SAR ADC with Noise Reduction
This SAR ADC supports 10-bit and 12-bit resolutions for sensor applications. A data-

driven noise-reduction technique improves comparator performance with low power increase. Fabricated in 65 nm CMOS, it achieves up to 10.1-bit ENOB while consuming only 97 nW.

14-bit 4-MS/s VCO-Based SAR ADC
A 14-bit VCO-based SAR ADC uses deep metastability for background mismatch calibration. Implemented in 40 nm CMOS, it achieves 78.7 dB SNDR and over 93 dB SFDR with very low power consumption and high energy efficiency.

0.5-V 12-bit SAR ADC with Adaptive Comparator
This low-voltage SAR ADC uses an adaptive time-domain comparator with noise optimization to reduce power consumption by 50%. Designed in 90 nm CMOS, it achieves up to 10.7-bit ENOB with excellent FoM performance at low supply voltage.

Low-Power SAR ADC Design Survey
This survey reviews low-power SAR ADC architectures, covering operation principles, error analysis, and modern energy-efficient techniques for comparators, DACs, and SAR logic in low-to-medium speed applications.

0.3-V 10-bit 3-MS/s SAR ADC for Biomedical Applications
An ultra-low-voltage SAR ADC for biomedical implants is presented. It uses comparator calibration and kickback noise reduction techniques to improve accuracy and efficiency. Fabricated in 90 nm CMOS, it achieves 9.08-bit ENOB with only 6.6 µW power consumption.

III. EXISTING METHOD

Voltage-mode comparators can be loosely classified into (i) static comparators, (ii) semi-dynamic comparators, and (iii) fully dynamic comparators. A static comparator consists of a pre-amplifier followed by a regenerative latch, both are static. These comparators enjoy a low kickback from the output, accredited to the isolation provided by the pre-amplifier between the input and output of the comparator. Static comparators, however, are not particularly suitable for power-constrained applications due to their non-zero static power consumption.

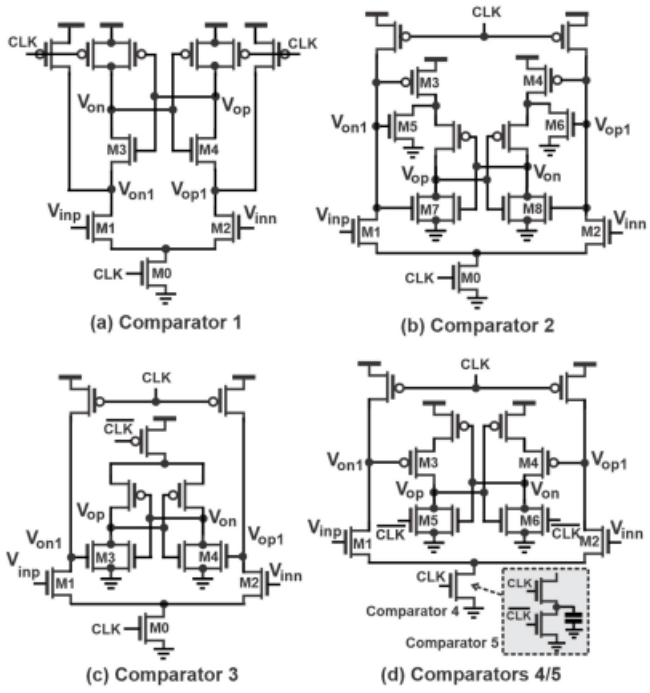


FIGURE. (a) Single-stage dynamic comparator (comparator 1)] and (b/c/d) two-stage dynamic comparators

The proposed comparator operates during reset phase (CLK=0) and evaluation phase (CLK=1) of the clock signal. When CLK = 0, the transistors MT1 and MT2 are turned OFF and both Fn and Fp terminals will be charged to Vdd through M3 and M4. Then the

transistors MI1 and MI2 are turned ON. The pass transistor SC shorts the output terminals Outp and Outn during the reset phase. The pass transistor SC shares the charge between two output terminals Outp and Outn, as one of the output terminal will be at Vdd and other at Gnd after the previous evaluation phase. Hence output terminals will be held at constant voltage level. When CLK = 1, the transistors MT2 and MT1 are ON and transistors M3 and M4 are OFF. Both Fn and Fp terminals will discharge at different speed which depends on the inputs applied to the circuit. If Vinp > Vinn, the terminal Fn discharges faster than Fp and vice versa. If the potential at terminals Fp or Fn, becomes less than the threshold voltage of transistor (MI2 or MI1), the transistor MI2 or MI1 turns OFF. The latch stage of the comparator drives, one output to Vdd and other output to ground. Thus input signals can be compared at quickly during evaluation phase. This greatly reduces the delay and power consumption in the circuit.

Disadvantage of Existing system

- High power consumption
- Limited speed performance
- Kickback noise issues
- Large chip area requirement
- Reduced accuracy at low voltage
- Higher offset voltage
- Sensitivity to PVT variations
- Increased circuit complexity
- Higher delay during comparison

IV. PROPOSED METHOD

A precharge-based comparator circuit, commonly referred to as a **dynamic comparator** or **latched comparator**, is a high-speed, low-power circuit used to compare two analog signals and output a digital signal (0 or 1). Unlike static comparators, these circuits use a clock signal to operate in two phases—precharge and evaluation—which eliminates DC power consumption and significantly reduces power dissipation, making them ideal for Analog-to-Digital Converters (ADCs), specifically Successive Approximation Register (SAR) ADCs.

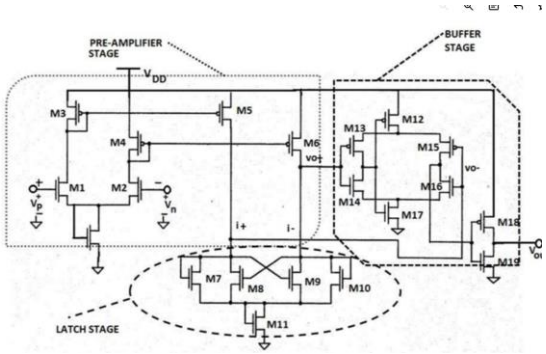
Operating Principle

The precharge-based comparator operates by switching between two states, primarily using MOS transistors as switches:

- **Precharge Phase (Clock = 0):** The output nodes and/or intermediate internal nodes are charged to a specific potential, usually

(or sometimes a lower voltage in partial precharging schemes to save power). The tail transistor is off, preventing current from flowing to ground.

- **Evaluation Phase (Clock = 1):** The precharge transistors are turned off, and a footer (tail) transistor turns on, allowing the output nodes to discharge based on the difference between the input voltages (and). The higher input voltage causes its corresponding output node to discharge faster, and a positive feedback latch strengthens this difference, producing a full-swing digital output.



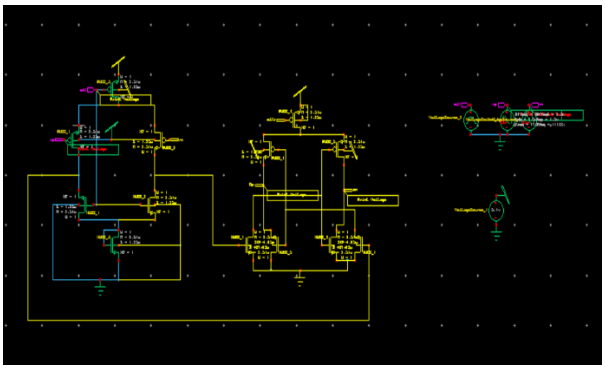
Advantages of Proposed System

- **Low Power Consumption:** Consumes power only during comparison operation.
- **High-Speed Operation:** Fast regenerative action enables quick comparison.
- **No Static Power Loss:** Eliminates continuous DC current flow.
- **Reduced Delay:** Provides faster output response.
- **High Accuracy:** Detects small input voltage differences effectively.
- **Compact Design:** Requires fewer transistors and smaller chip area.
- **Low-Voltage Operation:** Works efficiently at low supply voltages.
- **Energy Efficient:** Suitable for battery-powered applications.
- **Suitable for SAR ADCs:** Provides fast and reliable ADC performance.
- **Supports High Sampling Rates:** Operates efficiently at high frequencies.

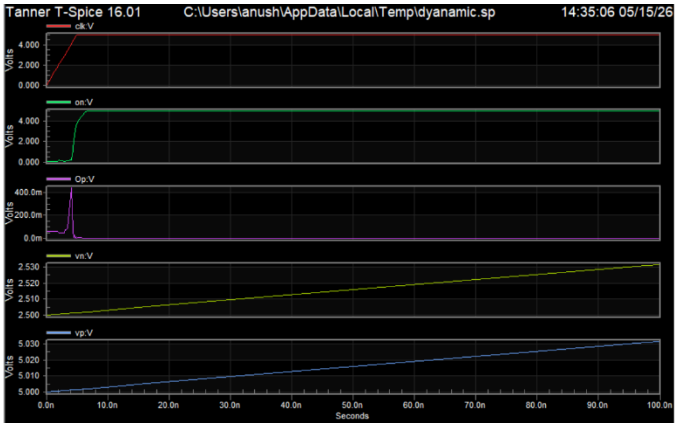
V. SIMULATION RESULTS:

Dynamic comparator

Schematic Design



Waveforms



Power

```
Max power 3.884398e-003 at time 2.90412e-009
Min power 1.728020e-007 at time 5.77559e-008
```

Time

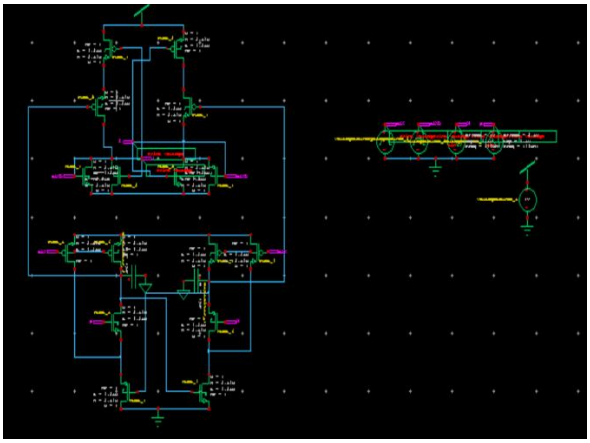
```
Parsing                          0.04 seconds
Setup                            0.07 seconds
DC operating point               0.10 seconds
Transient Analysis               0.01 seconds
Overhead                         1.17 seconds
-----------------------------------------------
Total                            1.38 seconds
```

Area (Size)

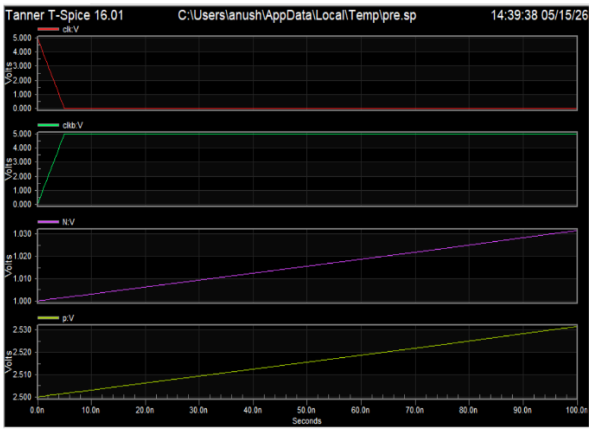
```
Device and node counts:
                MOSFETs -       13
   MOSFET geometries -        2
     Voltage sources -        4
          Subcircuits -        0
   Model Definitions -        2
     Computed Models -        2
   Independent nodes -        8
      Boundary nodes -        5
          Total nodes -       13
```

Charge Equalized Dynamic Comparator:

Schematic Design



Waveforms



Power

```
Power Results

VVoltageSource_5 from time 0 to 100
Average power consumed -> 3.680616e-015 watts
Max power 1.105064e-004 at time 5e-009
Min power 3.790234e-007 at time 1e-007
```

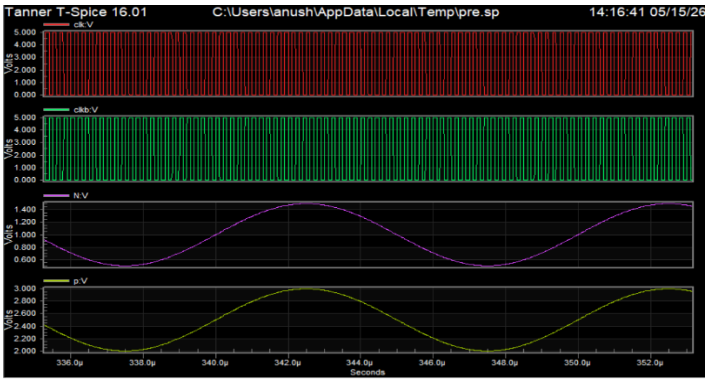
Time

```
Parsing                                 0.04 seconds
Setup                                   0.02 seconds
DC operating point                      0.11 seconds
Transient Analysis                      0.01 seconds
Overhead                                0.52 seconds
-----------------------------------------------------
Total                                   0.69 seconds
```

Area (Size)

```
Device and node counts:
                MOSFETs -       16
   MOSFET geometries -        2
          Capacitors -        2
     Voltage sources -        5
          Subcircuits -        0
   Model Definitions -        2
     Computed Models -        2
   Independent nodes -       11
      Boundary nodes -        6
          Total nodes -       17
```

Final Analog to Digital Converted Signal



Final Comparison Table

PARAMETER	DYNAMIC COMPARATOR	CHARGE EQUALIZED DYNAMIC COMPARATOR
AREA (SIZE)	13 nodes	17 nodes
TIME (DELAY)	1.38 seconds	0.69 seconds
POWER	3.884398e (Watts)	1.105064e (Watts)
SUMMARY	• Higher area • Higher delay • Higher power consumption	• Higher area (slightly) • Lower delay (faster) • Lower power consumption

VI. CONCLUSION

A critical review and the classification of comparators in low-power low-data-rate SAR ADCs were presented. Both voltage-domain and time-domain comparators were studied and their pros and cons were examined. The architecture, comparison time, and power consumption of five widely used voltage-domain dynamic comparators were studied first. It was followed with an investigation of kickback in these comparators. We showed although clock kickback is common-mode, the impedance asymmetry of the DAC of SAR ADCs arising from the different resistances of DAC switches gives rise to a differential clock kickback that occurs earlier than output kickback with more strength and hence dictates the kickback in dynamic comparators. If the strength and duration of clock kickback are sufficiently large, the comparator will yield an erroneous output. The dependence of clock kickback on the input of SAR ADC in LSB conversion was also investigated. The offset voltage of the dynamic comparators and its dependence on supply voltage were investigated, and the minimum tuning bits of digitally tuned offset compensation capacitor arrays were obtained. The noise of dynamic comparators was also investigated. The noise of dynamic comparators can be reduced by increasing the width of the input transistors at the price of more power consumption, worsening clock kickback, and the increased loading impact of the comparator on the DAC.

VII. REFERENCES

T. Matsuura, “Recent progress on CMOS successive approximation ADCs,” IEEJ Trans. Elect. Electron. Eng., vol. 11, no. 5, pp. 535–548, 2016.

[2] P. Harpe, “Successive approximation analog-to-digital converters: Improving power efficiency and conversion speed,” IEEE Solid-State Circuits Mag., vol. 8, no. 4, pp. 64–73, Nov. 2016.

X. Tang et al., “Low-power SAR ADC design: Overview and survey of state-of-the-art techniques,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 69, no. 6, pp. 2249–2262, Jun. 2022.

[4] P. Harpe, “Low-power SAR ADCs: Basic techniques and trends,” IEEE Open J. Solid-State Circuits Soc., vol. 2, pp. 73–81, 2022.

[5] S. Gambini and J. Rabaey, “Low-power successive approximation converter with 0.5 V supply in 90 nm CMOS,” IEEE J. Solid-State Circuits, vol. 42, no. 11, pp. 2348–2356, Nov. 2007.

[6] M. van Elzakker, E. van Tuijl, P. Geraedts, D. Schinkel, E. Klumperink, and B. Nauta, “A 10-bit charge-redistribution ADC consuming 1.9 µW at 1 MS/s,” IEEE J. Solid-State Circuits, vol. 45, no. 5, pp. 1007–1015, May 2010.

[7] D. Zhang, A. Bhide, and A. Alvandpour, “A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13-µm CMOS for medical implant devices,”

IEEE J. Solid-State Circuits, vol. 47, no. 7, pp. 1585–1593, Jul. 2012.

[8] S. Lee, S. Park, H. Park, and J. Sim, "A 21 fJ/conversion-step 100 kS/s 10-bit ADC with a low-noise time-domain comparator for lowpower sensor interface," IEEE J. Solid-State Circuits, vol. 46, no. 3, pp. 651–659, Mar. 2011.

[9] J. Cheong, K. Chan, P. Khannur, K. Tiew, and M. Je, "A 400-nW 19.5- fJ/conversion-step 8-ENOB 80-kS/s SAR ADC in 0.18-μ CMOS," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 58, no. 7, pp. 407–411, Jul. 2011.

[10] S. Haenzsche, S. Höppner, G. Ellguth, and R. Schüffny, "A 12-b 4-MS/s SAR ADC with configurable redundancy in 28-nm CMOS technology," IEEE Trans. Circuits Syst. II, vol. 61, no. 11, pp. 835–839, Nov. 2014.

[11] C. Liu, S. Chang, G. Huang, and Y. Lin, "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure," IEEE J. Solid-State Circuits, vol. 45, no. 4, pp. 731–740, Apr. 2010.

[12] D. Osipov and S. Paul, "Two-step monotonic switching scheme for low-power SAR ADCs," in Proc. IEEE Int. New Circuits Syst. Conf., 2017, pp. 205–208.

[13] S. Hsieh and C. Hsieh, "A 0.3-V 0.705-fJ/conversion-step 10-bit SAR ADC with a shifted monotonic switching procedure in 90-nm CMOS," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 63, no. 12, pp. 1171–1175, Dec. 2016.

[14] P. Lee, J. Lin, and C. Hsieh, "A 0.4 V 1.94 fJ/conversion-step 10 bit 750 kS/s SAR ADC with input-range-adaptive switching," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 63, no. 12, pp. 2149–2157, Dec. 2016.

[15] G. Huang, S. Chang, C. Liu, and Y. Lin, "A 1-μW 10-bit 200-kS/s SAR ADC with a bypass window for biomedical applications," IEEE J. Solid-State Circuits, vol. 47, no. 11, pp. 2783–2795, Nov. 2012.

[16] B. Nauta and A. Venes, "A 70-MS/s 110-mW 8-b CMOS folding and interpolating a/D converter," IEEE J. Solid-State Circuits, vol. 30, no. 12, pp. 1302–1308, Dec. 1995.

[17] A. Venes and R. van-de Plassche, "An 80-Mhz, 80-mW, 8-b CMOS folding a/D converter with distributed track-and-hold preprocessing," IEEE J. Solid-State Circuits, vol. 31, no. 12, pp. 1846–1853, Dec. 1996.

[18] P. Figueiredo and J. Vital, "Kickback noise reduction techniques for CMOS latched comparators," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 53, no. 7, pp. 541–545, Jul. 2006.

[19] J. Fang et al., "A 5-GS/s 10-b 76-mW time-interleaved SAR ADC in 28 nm CMOS," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 64, no. 7, pp. 1673–1683, Jul. 2017.

[20] P. Harpe, E. Cantatore, and A. van Roermund, "A 10b/12b 40 kS/s SAR ADC with data-driven noise reduction achieving up to 10.1b ENOB at 2.2 fJ/conversion-step," IEEE J. Solid-State Circuits, vol. 48, no. 12, pp. 3011–3018, Dec. 2013.

[21] S. D'Amico, G. Cocciolo, A. Spagnolo, M. D. Matteiso, and A. Baschirotto, "A 7.65-mW 5-bit 90-nm 1-Gs/s folded interpolated ADC without calibration," IEEE Trans. Instrum. Meas., vol. 63, no. 2, pp. 295–303, Feb. 2014. [22] H. Tang, Z. Sun, K. Chew, and

L. Siek, "A 5.8 nW 9.1-ENOB 1-kS/s local asynchronous successive approximation register ADC for implantable medical device," IEEE Trans. VLSI Syst., vol. 22, no. 10, pp. 2221–2225, Oct. 2014.

[23] N. Martin and R. Amirtharajah, "Improving SNDR and SFDR in capacitive DACs using match enhancement," in Proc. IEEE Int. Symp. Circuits Syst., 2019, pp. 1–5.