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Research Paper

Analysis and Improvement of Error-Tolerant in the Digital Systems by Using Static Segmentation of Multifunctional Multipliers

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Abstract –

The demand for energy-efficient and high-performance computing systems is continuously increasing due to the rapid growth of ubiquitous computing devices and the large volume of data that needs to be processed. Edge computing, for instance, requires fast data analysis near the data acquisition points to reduce response time and save bandwidth. At the same time, these systems must operate under strict power constraints, especially in battery powered embedded and mobile devices. The need for low-power and high-speed circuits has led to the development of new design paradigms. Approximate computing has emerged as a promising technique to achieve these objectives by sacrificing arithmetic accuracy in computation results. This approach is suitable for applications such as multimedia processing and machine learning, where a small loss in accuracy is acceptable. In recent years, approximate arithmetic circuits, particularly adders and multipliers, have been extensively studied because they are among the most power-consuming digital components. Several approaches have been proposed to design highly efficient approximate multipliers. In logarithmic multipliers, the product is obtained by adding approximate logarithms of the operands and then computing the antilogarithm of the result. Recursive multipliers use small elementary approximate multiplier blocks, typically of size 2×2 or 4×4, which are combined hierarchically. Multipliers based on approximate compressors or counters are designed to efficiently sum partial products. Truncated multipliers eliminate some of the least significant partial products, and the resulting truncation error is reduced using suitable correction functions. Genetic optimization algorithms have also been applied to explore the design space of approximate multipliers. In addition, approximate Booth multipliers have been proposed by various researchers. Customized approximate multipliers for efficient implementation of multiply accumulate (MAC) units have also been developed. These designs exploit error mitigation and correction techniques and combine the multiplier and adder into a unified approximate structure. An important class of approximate multipliers, known as segmented multipliers, extracts a set of m contiguous bits (an m-bit segment) from each of the two n-bit operands. These segments are multiplied using an internal m×m multiplier, and the resulting 2m-bit product is shifted appropriately to produce the final 2n-bit output. In this work, we investigate approximate multipliers based on static segmentation. In these circuits, a fixed set of m contiguous bits is extracted from each of the two n-bit operands. The extracted segments are applied to a small m×m internal multiplier, and its output is properly shifted to generate the approximate result. Both signed and unsigned multipliers are analyzed, and for unsigned multipliers, a new segmentation technique is proposed. We also introduce simple and effective correction techniques that significantly reduce approximation errors with minimal hardware overhead. A detailed comparison with previously proposed approximate multipliers is performed using a 28 nm technology implementation. The results show that static segmented multipliers with the proposed correction techniques lie on or close to the Pareto-optimal frontier for both power versus normalized mean error distance (NMED) and power versus mean relative error distance (MRED) trade-off curves. Therefore, these multipliers are promising candidates for applications where a certain level of error is acceptable. This conclusion is further supported by experimental results obtained from image processing and image classification applications.

Keywords – Booth multipliers, Approximate computing, Error-Tolerant.

1. INTRODUCTION

In the ever-evolving landscape of digital computing, the pursuit of efficiency and resilience against errors is paramount. One significant stride in this direction is the development of an innovative solution: an Ultra-Efficient Approximate Multiplier with Error Compensation. This cutting edge technology is designed to address the needs of applications where error resilience is of critical importance. The multiplier's distinctive feature lies in its explicit design for applications where error resilience is paramount. In sectors such as edge computing, Internet of Things (IoT), or critical embedded systems, mitigating errors without

compromising performance is a non-negotiable requirement. The Error Compensation mechanism embedded within the multiplier ensures that computational inaccuracies are effectively addressed, making it a robust solution for scenarios where precision is crucial. Approximation Precision: The multiplier strategically employs approximation techniques to balance precision and speed, optimizing computational efficiency. An Approximate Multiplier fundamentally operates on the premise that not all applications require absolute precision in multiplication. By strategically introducing controlled approximations in the multiplication process, these multipliers achieve a fine balance between computational accuracy and efficiency. This departure from the conventional pursuit of precise results enables significant gains in terms of speed, power consumption, and area utilization. Approximate Multipliers find applicability across diverse domains, ranging from signal processing to machine learning and embedded systems. In scenarios where a slight deviation from the exact product is acceptable, these multipliers shine. Applications in image and signal processing, for instance, can leverage the computational acceleration offered by Approximate Multipliers without sacrificing the quality of the end result.

2. EXISTING METHOD

The provided passage offers a comprehensive exploration of the landscape of approximate multipliers, with a specific focus on unsigned multipliers, as documented in the literature. An approximate multiplier, a cornerstone in digital circuitry, engages in multiplication with a deliberate introduction of imprecision, thereby opening avenues for potential energy savings and enhanced hardware efficiency. The discourse delves into the intricate domain of designing such multipliers, discerning between those without an Error Compensation Module (ECM) and those fortified with ECM to address and mitigate errors. The narrative unfolds with a meticulous examination of numerous prior works, each contributing distinct techniques to the evolving tapestry of approximate multipliers. Notably, attention is directed towards the first category, encompassing designs devoid of ECM. Within this realm, diverse strategies are unveiled, including the proposition of hybrid approximate multipliers hinging on a variety of compressors. These compressors, each with its unique characteristics, form the building blocks for crafting multipliers that tactically balance precision and efficiency. Furthermore, imprecise multipliers emerge as key players in constructing high-order multiplication circuits, harnessing the advantages of approximation for optimal performance. Compressors of varying orders also take center stage, showcasing the versatility of approximate multiplication methodologies. Additionally, the discussion touches upon the realm of approximate recursive multipliers, cleverly incorporating high-performance building blocks for heightened computational prowess. Logarithmic multipliers make a notable appearance, especially tailored for low-power error-tolerant applications, further expanding the spectrum of applications for approximate multiplication. The narrative gracefully transitions to the second approach, emphasizing designs integrating an error compensation module. These modules, crucial in their role, aim to identify and rectify errors introduced during the approximate multiplication process. The exploration of this avenue unveils a panorama of innovations, ranging from nuanced modifications to 4-2 compressor designs, fostering enhanced error resilience. Energy-efficient multipliers make their presence felt through the integration of modified compressors, contributing to a sustainable and power-conscious computing environment. Furthermore, the introduction of error recovery modules stands out as a testament to the commitment to robustness in the face of approximation-induced errors. In summation, this insightful passage not only navigates the intricate landscape of approximate multipliers but also serves as a gateway to a plethora of innovative designs and methodologies. It underscores the dynamism within the field, showcasing the evolution of approximate multipliers and their pivotal role in shaping the future of energy-efficient and high-performance digital circuitry. The traditional configuration of the 8-bit Dadda multiplier, commonly employed as the benchmark in prior studies, was elucidated. In three hybrid approximate multipliers were introduced, each utilizing distinct approximate compressors characterized by varying levels of accuracy and performance. proposed two imprecise 4 × 4 multipliers, strategically employed to construct a higher-order multiplier. Introduced compressors of different orders with consistent output weights for use in approximate multipliers. Presented approximate recursive multipliers founded on high-performance building blocks. Explored approximate multipliers employing static segmentation coupled with error correction methods. suggested logarithmic multipliers tailored for low power, error-tolerant applications. In a novel adaptation to the approximate 4-2 compressor design and the proposal of an error recovery module were outlined. Introduced an energy efficient approximate multiplier utilizing a modified 4:2 compressor and suggested an error recovery module capable of detecting erroneous conditions. Put forth three inventive approximate 4-2 compressors incorporated into 8-bit multipliers. Concurrently, an Error Compensation Module (ECM) was introduced to enhance the accuracy of the approximate multiplier. Presented an unsigned approximate multiplier architecture founded on truncation and approximation, aiming to optimize hardware without substantial sacrifices in accuracy. This design streamlined partial products in the central section through 4:2 approximate compressors, with

the introduced error compensated by an efficient ECM. Notably, the primary segment of the multiplier retained exact logic implementation.

Demerits

While the passage highlights the advantages and innovations in the realm of approximate multipliers, it's important to acknowledge that, like any technology, they come with certain disadvantages and challenges. Here are some potential
drawbacks to consider:

Loss of Precision:

The primary trade-off with approximate multipliers is the intentional introduction of imprecision. While this imprecision may be acceptable for certain applications, it can lead to a loss of precision in calculations. This drawback might limit the suitability of approximate multipliers in applications where high precision is critical.

Impact on Accuracy:

In applications where accuracy is paramount, such as scientific computations or financial calculations, the imprecision introduced by approximate multipliers could lead to unacceptable errors. This limitation might constrain the use of approximate multipliers in contexts where precise results are non-negotiable.

Application Dependency:

The effectiveness of approximate multipliers depends heavily on the specific application. While they may excel in scenarios where a certain level of imprecision is tolerable, their performance might be suboptimal or even detrimental in applications that require absolute accuracy.

Increased Design Complexity:

The integration of Error Compensation Modules (ECMs) adds a layer of complexity to the design. ECMs aim to rectify errors introduced during the approximate multiplication process, but their implementation can increase the overall complexity of the circuitry, potentially impacting the ease of design and verification.

Limited Applicability:

The advantages of approximate multipliers may not be universally applicable. Certain applications or industries may prioritize precision over computational efficiency, limiting the scope of where these innovative multipliers can be effectively employed.

3. PROPOSED METHOD

The conventional setup of the 8-bit Dadda multiplier, frequently used as a standard in previous research, was clarified. In three hybrid approximate multipliers were introduced, each employing distinct approximate compressors characterized by varying degrees of accuracy and performance. Suggested the use of two imprecise 4 × 4 multipliers strategically to construct a multiplier of higher order. Brought forth compressors of different orders with consistent output weights for application in approximate multipliers. Showcased approximate recursive multipliers built upon high-performance building blocks. Investigated approximate multipliers that incorporated static segmentation
along with error correction methods. The proposed logarithmic multipliers tailored for applications demanding low power and error tolerance, whereas recommended dynamic range approximate logarithmic multipliers for machine learning applications, acknowledging a trade-off between higher error and lower energy consumption. In a fresh adaptation to the design of the approximate 4-2 compressor and the introduction of an error recovery module were delineated. Introduced an energy-efficient approximate multiplier that utilized a modified 4:2 compressor and suggested an error recovery module capable of detecting erroneous conditions. Introduced three innovative approximate 4-2 compressors integrated into 8-bit multipliers. Simultaneously, an Error Compensation Module (ECM) was introduced to augment the accuracy of the approximate multiplier. Outlined an unsigned approximate multiplier architecture grounded in truncation and approximation, with the goal of optimizing hardware without significant compromises in accuracy. This design streamlined partial products in the central section through 4:2 approximate compressors, with the introduced error being compensated by an efficient ECM. Remarkably, the primary section of the multiplier maintained exact logic implementation. Initially, to generate an accurate output for the "0000" combination, which is likely to occur at the input, the outputs are zeroed. Subsequently, the negative Exclusive Differences (EDs) associated with inaccurate inputs are effectively utilized in crafting an efficient error compensation module. A noteworthy aspect of this approach is that, as per this scheme, the ED corresponding to each input equals the number of '1's in that input. In this context, states with higher EDs are less probable to occur. Assuming uniform distribution of input bits in a multiplier, where each input bit has an equal probability of being '0' or '1', the probability of a partial product (generated by a 2-input AND gate) equalling '1' ('0') is 1/4 (3/4). Consequently, the probabilities of inputs having zero, one, two, three, and four '1's are 31.5%, 10.5%, 3.5%, 1.1%, and 0.4%, respectively.

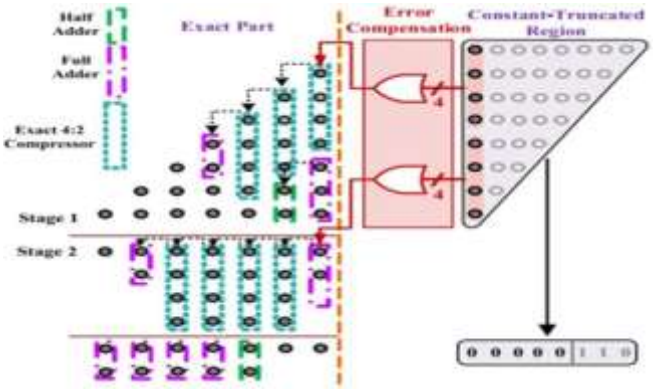

Fig. 1: Partial product reduction of the proposed approximate multiplier.

In light of this, the proposed error compensation module is tailored to address errors stemming from cases with higher occurrence probabilities. Additionally, the output corresponding to the input "0000" remains uncorrupted. To achieve this, two 4-input OR gates, totaling 20 transistors, are employed. By performing a logical OR operation on the four inputs, the errors corresponding to highlighted cells in Table I are identified. Subsequently, by utilizing the output of the OR gates as the Carry input for compressors in the subsequent stage, the impact of negative EDs is significantly mitigated. It is pertinent to note that the exclusive presence of negative EDs aligns well with neural network applications, particularly due to the ReLU activation function. While the least significant columns are typically truncated for enhanced hardware efficiency, this may result in a relative loss of accuracy, which can be compensated. Accordingly, the three Least Significant Bits (LSBs) of the products are replaced with a constant correction term of "110" (decimal value of 6) to improve accuracy. This correction term is computed as an average value of input combinations in the least significant columns. This simplification leads to the omission of 28 two input AND gates from the partial production stage, along with numerous adder and compressor circuits in the subsequent stages.

Proposed System Merits & Applications

Approximate multipliers offer several advantages, making them valuable in certain applications where a degree of imprecision is acceptable. Here are some key advantages of approximate multipliers:

Computational Efficiency:

Approximate multipliers prioritize computational speed over absolute precision. By relaxing the requirement for exact results, they can perform multiplication operations more rapidly than traditional, more precise multipliers. This is particularly advantageous in applications where real-time processing and speed are critical.

Energy Savings:

The intentional introduction of imprecision in approximate multipliers often results in reduced power consumption. By compromising on precision to some extent, these multipliers can achieve energy efficiency, making them suitable for battery-powered devices, IoT (Internet of Things) applications, and other energy-constrained systems.

Hardware Resource Optimization:

Approximate multipliers can be designed to use fewer hardware resources compared to their precise counterparts. This reduction in hardware complexity leads to smaller chip area requirements, lower costs, and improved scalability in designs with limited resources.

Application-Specific Customization:

The level of approximation in these multipliers can be tailored to suit specific applications. This customization allows designers to strike a balance between computational accuracy and efficiency, making approximate multipliers versatile for a wide range of tasks.

Error-Tolerant Applications:

In scenarios where a certain level of imprecision is tolerable, such as in machine learning applications with error-tolerant algorithms, approximate multipliers can provide satisfactory results. They contribute to the development of robust systems where minor inaccuracies do not compromise overall performance.

Applications:

Approximate multipliers find applications in various domains where a certain degree of imprecision is acceptable, and computational efficiency and energy savings are prioritized. Here are some key applications of approximate multipliers

Machine Learning and Neural Networks:

In machine learning applications, especially those involving neural networks, approximate multipliers can be employed. These algorithms often exhibit resilience to minor errors, and the computational efficiency of approximate multipliers aligns well with the parallel processing requirements of neural networks.

Digital Signal Processing (DSP):

DSP applications, such as audio and image processing, often involve repetitive and computationally intensive tasks. Approximate multipliers can be utilized in these scenarios to accelerate processing speed, making them suitable for real-time applications like speech recognition, image classification, and audio processing.

Internet of Things (IoT) Devices:

IoT devices operate in resource-constrained environments where energy efficiency is crucial. Approximate multipliers can help reduce power consumption, extending the battery life of IoT devices without significantly compromising their functionality.

Edge Computing:

In edge computing environments where computational tasks are performed locally on devices rather than in a centralized

cloud, approximate multipliers contribute to faster processing and reduced energy consumption. This is particularly relevant for applications requiring quick decision-making at the edge.

Wireless Communication Systems:

In wireless communication systems, such as those used in mobile devices and wireless sensors, energy efficiency is a critical consideration. Approximate multipliers can be employed to reduce power consumption in signal processing tasks without sacrificing overall system performance.

4. SIMULATION RESULTS

Implementing clock getting in our proposed design has the potential to diminish certain parameters, such as power consumption or dealy.

Fig.2: Simulation Waveform of Proposed Approximate Multiplier.

Developing an ultra – efficient approximate multiplier with error compensation is crucial for balancing computational accuracy and energy consumption in designed circuits. The challenge includes optimizing energy efficiency while maintaining acceptable precision for error resilient applications like signal processing and machine learning. The resulting multiplier shows dynamically adopt its approximation level to meet the specific requirements of diverse applications.

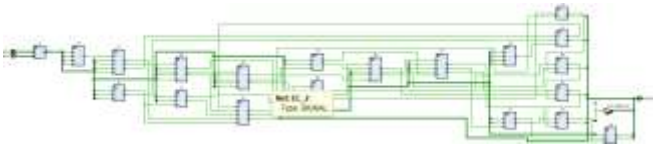

Fig.3: RTL Schematic of Proposed Approximate Multiplier.

The exact full adder and exact 4:2 compressor of the proposed
approximate multiplier architecture are described and compared to previous designs.

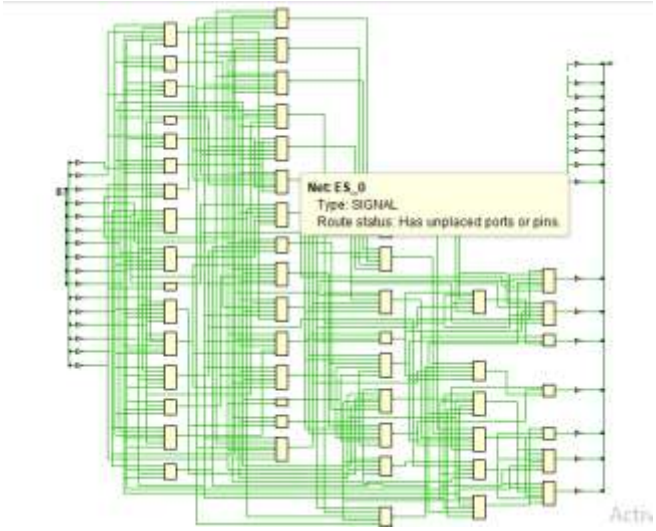

Fig.4: Technology Schematic of Proposed Approximate Multiplier.

Name	Slice LUTs (134600)	Bonded IOB (400)
PROPOSED_APPROXIMATE_MULTIPLIER	47	32

Table:1 Area of Proposed Approximate Multiplier

Power estimation from synthesized netlist. Activity derived from constraints files, simulation files or vector less analysis. Note: these early estimates can change after implementation.

Name	Slack	High Fanout	From	To	Total Delay
Path 1		17	b[7]	z[13]	7.764

Table: 2 Delay of Proposed Approximate Multiplier

CONCLUSION

This brief proposes an ultra-efficient approximate multiplier, including a constant-truncated region, an error correction module, and an exact part. Ignoring the outputs in the truncated region is equivalent to using a 4:2 approximate compressor with outputs equal to zero. Accordingly, it leads to an accurate output for the “0000” input, which is most likely to occur. Moreover, the EDs of the other inputs become negative. As the absolute ED corresponding to each input equals the number 1’s in that input, the input with a higher ED has a lower probability of occurrence. Accordingly, an efficient ECM is proposed to compensate for the errors resulting from the most probable cases to a large extent. Also, the existence of entirely negative EDs can be more efficient for NN applications due to the functionality of the ReLU activation function. Accordingly, the proposed design can be an effective alternative for exact multipliers in practical error-resilient applications.

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