ISSN 2319-5991 www.ijerst.com

Peer Reviewed, Referred & Indexed Journal

Research Paper

A CMOS FULLY INTEGRATED OPTICAL WIRELESS POWER TRANSFER SOC FOR BIOMEDICAL IOT DEVICES

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ABSTRACT: This paper reports on the design and experimental characterization of a fully integrated optical wireless power transfer for biomedical internet-of-things devices. The solution has been fabricated on-chip in TSMC 0.18 µm standard Si CMOS technology within an area of 0.466 mm2 integrating a 500×500 µm2 Si photodiode. If compared with the solutions using different methodologies, optical wireless systems allow for reaching the highest electromagnetic compatibility with the further advantage of transferring electrical power from long distances. The architecture employs inverter stages to maximize the value of the achievable output voltage starting from the input voltage and currents provided by the integrated photodiode. The electrical and optical characterizations of the fabricated device were performed under both continuous and pulsed operation modes. Depending on the impedance of the external load to be powered, output voltages up to 2.45 V have been obtained from an input voltage of 0.35 V with an energy conversion efficiency of 58 %. The comparison of the main features achieved with those of similar solutions reported in the Literature has been performed. By employing low input voltages, the proposed system requires a reduced Si area, works at a lower clock frequency, achieves the higher output voltages to supply external loads with satisfactory output currents and good energy conversion efficiencies.

INDEX TERMS Biomedical systems, CMOS integrated photodiode, implantable devices, optical wireless power transfer.

I. INTRODUCTION

The rapid proliferation of Internet-of-Things (IoT) and intelligent IoT applications has created a growing demand for next-generation sensors and actuators. These solutions are equipped with wireless power and data transmission capabilities to overcome the limitations associated with battery powered solutions [1], [2], [3], [4], [5], [6], [7], [8], [9], [10]. Wired connections are hindered by challenges related to accessibility in diverse environments. Furthermore, the size of conventional batteries poses a significant bottleneck in the quest to reduce the footprint of IoT sensors, and the need for battery replacement compounds the downsides of such power sources [5], [6]. Consequently, there is an escalating need for diversified energy sources to power IoT devices. In response to these challenges, researchers are exploring various energy harvesting techniques to enable long-lasting, self-maintained IoT devices. Among the commonly employed methods, such as radio frequency (RF), thermal, and motion, one particularly promising avenue is optical energy harvesting [8], [9]. The utilization of optical energy harvesters, in fact, offers unique advantages, given their ability to convert ambient light into electrical power and transfer electrical power from long distances [10], [11], [12], [13], [14]. A specifically rapidly expanding field is the development of biomedical IoT systems, also known as Internet-of Medical-Things (IoMT) [15], [16], [17], [18], [19], [20]. In these systems, the use of Wireless Power Transfer (WPT) technology is intended primarily for integrated implantable systems [10], [11], [19], [21], [22], [23], [24], [25], [26], [27] designed for real-time health monitoring or therapeutic purposes. They need various sensors and custom-designed, low-voltage, low-power electronic front-end circuitries to accomplish signal acquisition and processing as well as data transfer from outside to inside a patient's body and vice versa [28], [29], [30], [31], [32], [33], [34]. Implantable systems, like pacemakers, deep brain stimulators, and cardiac monitoring sensors, operate using miniaturized in-situ long-life batteries that must be periodically replaced by surgery to guarantee the patient's health with possible unexpected risks such as infections. Several non-radiative wireless approaches have been proposed to power miniaturized implants [35], [36]. Magnetic coupling WPT solutions demonstrate relatively high efficiency, but for limited distances and RF-based methods suffer for low energy efficiencies and electromagnetic disturbances [21], [22], [23], [25], [37], [38]. Within this research framework, optical WTP (OWPT) architectures have been recognized as promising since optical technologies present a series of advantages [39], [40], [41], 1) the power transfer can be effective even at a long distance from the user (i.e., the patient in biomedical applications); 2) together with power transfer capability, optical-based systems allow also for data acquisition, processing, and transmission [28], [29], [41], [42]; 3) the light frequency of the order of 1014 Hz preserves the systems from induced electromagnetic disturbances to and/or from other neighbouring instrumentations so guarantying the highest level of electromagnetic compatibility; 4) the capability to operate with visible and near-infrared light of the environment or of that one generated by LEDs and semiconductor lasers [20], [39], [43]; 5) the possibility to implement bidirectional power and data transfer by means of special designed devices and architectures [28], [44], [45]. Moreover, in OWPT systems, photodiodes (PD) convert light power into an electrical current. However, the associated output voltage is not sufficient to power an implantable IoT device without the use of a suitable DC-DC converter. In this regard, the here proposed OWPT system is composed of an integrated PD, a ring oscillator, a clock buffer, and a charge pump. This solution was designed at transistor level and fabricated on-chip in TSMC 0.18 μm standard Si CMOS technology. The reported OWPT electronic architecture is based on standard CMOS inverter stages and the capacitors of the four-stage cross-coupled-based CP have been fully integrated. Summarizing, the main novelties of the presented solution are: 1) the capability to generate high output voltages and currents to supply external loads with good energy conversion efficiencies starting from small input voltages and operating with a low clock frequency by means of a proper integrated microelectronic design at transistor level (i.e., sizing and biasing); 2) the development of fully integrated solution (PD and electronic circuitry, including capacitors and clock source without the use of further external components and devices) requiring the smallest Si area with respect to other similar on-chip solutions, in particular, the required total Si area is only 0.466 mm2 ; 3) the possibility to operate in continuous and pulsed regimes; 4) with respect to both the preliminary work introducing the OWPT system design and its characterization through post-layout simulations [13] and all the other similar solutions in the Literature, electrical and optical full experimental characterizations have been performed (of only the electronic circuitry and the PD, as well as of the overall integrated system) also by employing an external light source and porcine skin emulating the human skin and under different operating conditions (e.g., different loads, input voltages and light intensities as well as in continuous and pulsed regimes).

II. LITERATURE REVIEW:

Sang-Woo Jun_, Ming Liu et.al[1], has implemented a novel high-performance storage architecture, which is named as BlueDBM (Blue Database Machine). This architecture can be used for scalable distributed flash and this aims at achieving high performance, high-capacity storage element which allow random access to the flash. Through this design throughput achieved is high as large number of flash chips are shared which has low latency. The authors have designed flash controllers which manages the chip-to-chip network with the help of Ethernet. The controller is placed between the storage element i.e., flash and the host this leads to hardware acceleration so latency gets directly reduced. The interface used for data transfer is PCIe. The designed storage architecture was implemented for Big Data applications where a communication link was established directly between nodes through flash controllers. The flash controllers accelerate the system.

Kermin Fleming et.al.[6] presents Customarily, equipment outlines divided over numerous FPGAs have had low execution because of the wastefulness of keeping up by every cycle timing in between discrete FPGAs. In this thesis, the authors have presented a system by which complex plans might be productively furthermore, naturally parcelled among numerous FPGAs utilizing expressly modified inertness obtuse connections. They portray the programmed amalgamation of a range proficient, elite system for directing these between FPGA joins. By mapping a different arrangement of vast research models onto a different FPGA stage, we illustrate that our device acquires critical additions in outline attainability, accumulation time, and even divider clock execution.

Yeonseung Ryu et.al., [9] the creators have composed another glimmer interpretation layer (FTL) plan called sifting FTL (FFTL). A FTL is an item or firmware executed inside the flash-based capacity. To duplicate a square utilizing flash memory, a FTL gives some inside functionalities, for instance, address elucidation, dreadful piece organization, wear levelling, and misstep update code checking. A FTL gets read and compose requests from the system and maps a shrewd area to a physical area in the NAND. The key part of a FTL is to redirect each compose requesting to a void zone of flash memory, thus keeping up a vital separation from the "destroy before-compose”. The new Filtering FTL called FFTL as an essential goal to channel metadata redesigns from information squares and data is overhauled to the page level plan. In the FFTL plan, the area elucidation of a square is ordinarily performed by however is performed by a page-level arrangement when the piece is updated.

Yang Ou et.al et.al [10] have passed on the flexible multichannel Flash memory controller engineering which can mishandle the parallelism of different chips. It bolsters all the burst operations, and helps the execution by reliably going on various gets to among various chips while utilizing the foul up correction code to redesign its dependability. The segments of the multi-channel parallel controller are embraced by far coming to of workloads. The makers demonstrated another adaptable multichannel parallel NAND streak memory controller arrangement. It underpins all the burst operations while utilizing the misstep change code to update its unwavering quality. In addition, recollecting the completed target to update as far as possible, the misuse of multichannel parallelism the structure produces dynamic trading approach for the mapping table in the FTL.

III. EXISTING METHOD

The solution is composed of an integrated square PD with an area of 500 × 500 μm2 and three sub-systems: (i) a ring oscillator (i.e., the ROS block) that generates a square wave whose frequency and amplitude depend on the continuous input voltage VIN ; (ii) a charge pump (i.e., the CP block) that provides the OWPT output voltage VOUT ; (iii) a driver circuit (i.e., the BUFFER block) that provides two square wave output signals CLKCP and /CLKCP, in phase opposition condition as shown in Fig. 1.

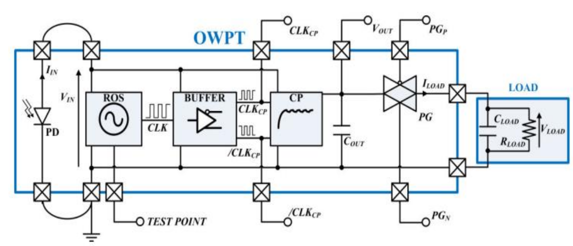


FIGURE 1. Overall block scheme of the proposed integrated OWPT system-on-chip.

Finally, PG is a standard pass-gate switch that allows to connect or disconnect the OWPT system from an external LOAD. To perform independently the electrical and optical characterizations of the OWPT system, the SoC external pads shown in Fig. 1 allow to connect/disconnect the integrated PD to/from the OWPT circuitry as well as the PG to/from the external LOAD. Moreover, the TEST POINT pad is used to verify and externally adjust/regulate the ROS block, while the PGP, PGN pads are employed to externally control the PG.The OWPT circuitry has been implemented by using a standard inverter-based circuit topology precisely designed at the transistor level in TSMC 0.18 µm standard Si CMOS technology in the Cadence Virtuoso environment, considering the specific requirements of each constitutive block. In the following, the functionalities of the OWPT blocks have been articulated, specifying the width W and length L of each employed transistor as well as the values on the integrated capacitors.

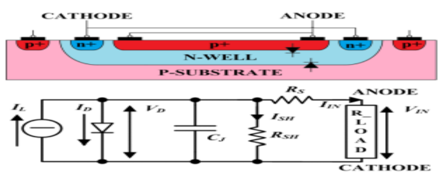


FIGURE 2. Upper Panel: physical structure of the integrated PNP PD; Lower Panel: equivalent electrical circuit of the PD.

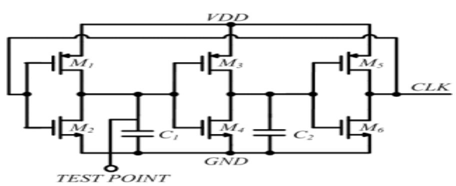


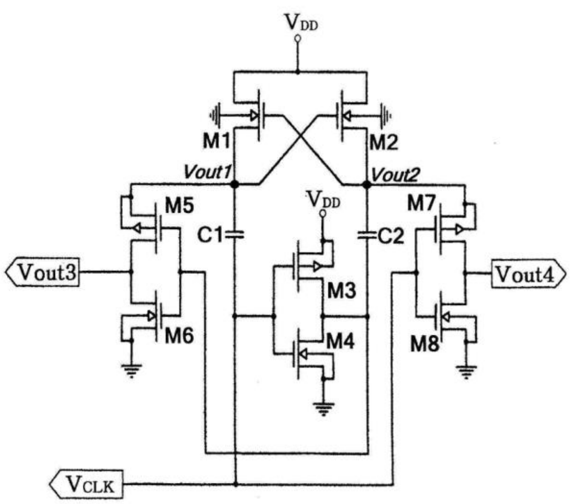
FIGURE 3. Schematic circuit of the ROS block.

Disadvantage of Existing system

- Conventional wireless power transfer methods such as RF and magnetic coupling suffer from limited transmission distance or low efficiency.
- Many existing designs require external components (like large photodiodes, power supplies, or clock sources), increasing system complexity.
- Some charge pump circuits experience voltage losses due to effects like body effect, reducing output performance.
- Existing solutions often need larger silicon area, making them less suitable for compact biomedical devices.
- Several systems show lower output voltage and current, which is insufficient for practical implantable applications.
- Lack of complete real-time testing under practical conditions limits their reliability.

IV. PROPOSED METHOD

Hysteretic and protreptic devices are bi-stable and their interstate switching depends on triggering voltages. Conventionally, devices can be classified to work as either hysteretic or I protreptic. This thesis proposes the first attempt to describe a circuit that switches between two opposite characteristics of hysteresis and progenesis to present a new circuit called Prophy's switch. The output of prophy's switch demonstrates a limited amount of randomness in its first cycle of operation and this factor is a strong reason to employ a prophy's switch for designing a Physical unclonable Function (PUF). In recent times PUF's has gained immense popularity for securing the IC's by providing unique identification code to each chip. The key design parameters of a PUF are uniqueness and reliability and designing a highly efficient PUF with optimal values of uniqueness and reliability is quite a challenge. Reliability depends on the chip's ability to resist changes to supply voltage and temperature variations, whereas, uniqueness depends on process variations during chip fabrication. Multiple PUF designs that employ reliability enhancement circuits and security algorithms achieve these design characteristics. Nonetheless, these techniques are design overheads. Finally, this thesis presents a novel PUF based on the prophy's switch called the prophy's PUF. The proposed prophy's PUF befittingly satisfies both uniqueness and reliability criteria, without any additional circuitry or security algorithms.



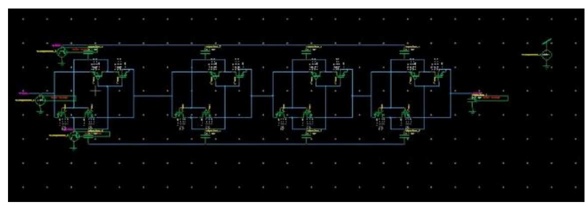
Advantages of Proposed System

- The proposed system operates with **very low input voltage (as low as 0.35 V)**, making it suitable for energy harvesting.
- It achieves **higher output voltage (up to 2.45 V)** with improved efficiency (~58%).
- Fully integrated design eliminates the need for **external components**, reducing size and complexity.
- Requires **very small chip area (0.466 mm²)**, ideal for biomedical and implantable devices.
- Works at **low clock frequency**, resulting in reduced power consumption.
- Supports both **continuous and pulsed operation modes**, making it versatile for different applications.

V. SIMULATION RESULTS:

The final designed circuit (multi-stage cross-coupled charge pump) successfully boosts a low input voltage to a higher output voltage through cascaded stages. Each stage incrementally increases the voltage using clock-driven switching, resulting in an amplified DC output.

5.1 Simulation Circuit



The proposed CMOS fully integrated Optical Wireless Power Transfer (OWPT) system operates with a minimum input voltage of **0.35 V** and achieves a maximum output voltage of **2.45 V**. In continuous mode, it provides stable output for ultra-low power loads, while in pulsed mode it delivers up to **52.5 µA** with the output dropping to **1.8 V**. The system operates at approximately **244 kHz** and reaches steady state within **400 ms**. An energy conversion efficiency of **58%** is achieved within a compact chip area of **0.466 mm²**, demonstrating its suitability for low-power biomedical IoT applications.

5.2 Graphical Representation

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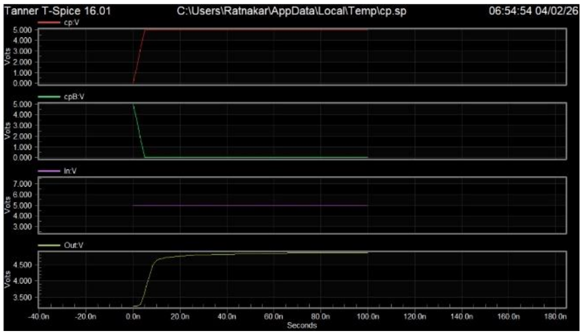

VI. CONCLUSION

This study reports on the design, fabrication and characterization of a fully integrated optical wireless power transfer system-on-chip designed for biomedical IoT devices. With respect to other solutions based on radiative and non-radiative techniques, optical systems attain the highest electromagnetic compatibility and transfer electrical power to external devices from long distances using environmental light and/or LED. The proposed solution was designed at the transistor level and fabricated on-chip in TSMC 0.18 µm standard Si CMOS technology using inverter stages to maximize the value of the achievable output voltage. The fabricated ASIC includes a 500 × 500 µm2 Si photodiode that provides the input current and voltage of the system. The employed Si area of the entire system is about 0.466 mm2 . The functionality of the fully integrated system-on-chip was experimentally verified by a complete electrical and optical characterizations evaluating the output voltage as a function of the impedance of the external device to be powered for various input voltage values. With a minimum input voltage of 0.35 V, the system can provide output voltages up to 2.45 V with the best energy conversion efficiency of about 58 %. The fabricated system has been also tested by performing measurements employing an external light source and porcine skin emulating the human skin as well as under both continuous and pulsed time mode operations, demonstrating its ability to be employed in different practical biomedical IoT applications. The achieved main characteristics of the presented integrated system were compared with those of similar solutions in literature. The comparison demonstrates that the proposed system requires a reduced Si area, works at a lower clock frequency, attains higher output voltages to supply external loads with adequate output currents and good energy conversion efficiencies.

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