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IMPLEMENTATION OF VEDIC MULTIPLIER USING CARRY TREE ADDERS

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ABSTRACT

The "Implementation of Vedic Multiplier using Carry Tree Adders" project represents a presentation for the growing importance of the efficient multipliers in the fields of Digital signal Processing, Designing of FPGA's , and other applications.

Multiplication is an important function in arithmetic operations. A CPU (central processing unit) devotes a considerable amount of processing time in performing arithmetic operations. Multiplication requires substantially more hardware resources and processing time than addition and subtraction. Digital signal processors (DSPs) are the technology that is omnipresent in engineering Discipline. Fast multiplication is very important in DSPs for digital filter, convolution, Fourier transforms etc Many Digital signal processing (DSP) systems includes multipliers as one of core hardware blocks. Multipliers hold a significant role in various DSP applications such as digital filtering, digital communication and Fast Fourier transform.

Vedic multiplier is implemented in this project with various types of adders to optimize the various parameters. The multiplier is a basic building block in Standard Digital Signal Processors (DSP). Most of the DSP tasks require real-time processing with several multiplications. Multiplication is most important arithmetic operation having wide applications from normal multiplication in DSP.

Multiplication process is used in many applications like instrumentation and measurement, communications, audio and video processing, animations, special effect, Graphics, image enhancement, Navigation, radar, GPS, and control applications like robotics, machine vision. Multiplication is the process of adding a number of partial products. Multiplication algorithms differ in terms of partial product generation and partial product

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addition to produce the final result.

Higher throughput arithmetic operations are important to achieve the desired performance in many real time signal and image processing applications. With time applications, many researchers have tried to design multipliers which offer either of the following- low power consumption, high speed, regularity of layout and hence less area or even grouping of them in multiplier. We use two different adders like ripple carry adder and hancarlson adder to compare their performance in terms of power , area utilization and time delay caused by those adders to decide the efficient adder for a vedic multiplier.

INTRODUCTION

Vedic Mathematics is a book written by Jagadguru Shankaracharya Bharati Krishna Trithaji Maharaja. The book includes 16 sutras which are said to be derived from 'Ganita sutras' of atharva veda. The principles of Vedic mathematics can be directly implemented in problems related to trigonometric functions, differential and integral calculus, plane and sphere geometry, conics and different methods of applied mathematics.

It covers explanation of several modern mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus. The beauty of Vedic mathematics lies in the fact that it reduces the otherwise cumbersome-looking calculations in conventional mathematics to a very simple one. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works.

The system is based on 16 Vedic sutras or aphorisms, which are actually word formulae describing natural ways of solving a whole range of mathematical problems.Out of the 16 sutras, we use 'urdhva tiryakbhyam' which indicates vertical-cross method of multiplication. This method reduces the Partial Products thus reducing the Power Consumption, Time delay and Area Utilization. This project also concentrates on choosing the efficient adder for the Multiplication , by comparing the Ripple carry adder and Hancarlson Adder.

We use Xilinx Vivado Software with Verilog Hardware Description Language (HDL) to design the 2 bit Vedic Multiplier and then the 4-bit Vedic Multiplier. These Multiplier Circuits consists of the Adder Blocks and are Designed according to the Vertical - Cross (Urdhva - Tiryakbhyam) method as discussed earlier. In the First stage Ripple Carry Adders are used and are replaced with the Hancarlson Adder in the Second Stage to compare the Parameters like

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Time Delay, Power Consumption and Area Utilization for Selecting the Efficient Adder for the Vedic Multiplier.

OBJECTIVE OF THE PROJECT

The primary objective of this project is to Design a Vedic Multiplier using the Xilinx Vivado Software and Verilog Hardware Description Language(HDL). Multipliers are important block in digital systems and play a critical role in digital designs. Along with accuracy demand for minimizing time area, power, and delay of the processor by enhancing speed is the focus point. This Project also Focusses on selecting an Efficient Adder for the Multiplier by Comparing Ripple carry and Parallel Prefix Adders. Vedic mathematics rules and Algorithms generate partial products concurrently and save time.

LITERATURE SURVEY

Search Academic Databases: Utilize academic databases like IEEE Xplore, Google Scholar, Scopus, and ACM Digital Library.

Review Recent Publications: Focus on recent publications (last 5-10 years) to ensure you're accessing the most up-to-date research in the field. Pay attention to articles that have been cited frequently, as they often represent seminal works.

Check Journals and Conferences: Look for articles in relevant journals (e.g., IEEE Transactions on A regular layout for parallel adders) and conference proceedings (e.g., IEEE International Conference on A Taxonomy of Parallel Prefix Networks).

Browse Theses and Dissertations: Explore theses and dissertations from universities worldwide. Search for terms like " vedic multiplier ," " carry tree adders ," "parallel prefix adders," etc., in online repositories like ProQuest Dissertations & Theses Global or institutional repositories ofuniversities.

Review Technical Reports and Whitepapers: Check technical reports and whitepapers published by robotics companies, mining industry organizations, and research institutions. Websites like arXiv and ResearchGate can be useful for accessing preprints and technical documents.

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The Proposed system involves the Survey of the different journals and Publications which explain the following studies . R.P.Brent and H.T. Kung, "A regular layout for parallel adders," IEEE Trans explains that With VLSI architecture, the chip area and design regularity represents a better measure of cost than the conventional gate count. It shows that addition of n-bit binary numbers can be performed on a chip with a regular layout in time proportional to log n and with area proportional to n.

D. Harris, "A Taxonomy of Parallel Prefix Networks," in Proc. 37th Asilomar Conf. Signals Systems and Computers: This literature describes about, Parallel prefix networks are widely used in high-performance adders. This paper also presents a three-dimensional taxonomy that not only describes the tradeoffs in existing parallel prefix networks but also points to a family of new networks. Adders using these networks are compared using the method of logical effort. The new architecture is competitive in latency and area for some technologies.These designs impose significant area and performance overheads.

T. Lynch and E. E. Swartzlander, "A Spanning Tree Carry Lookahead Adder," IEEE Trans. on Computers In this paper, we propose DFT modifications for cellular CLA adders to achieve complete CFM testability with special emphasis on the minimum impact in terms of area and performance.

Complete CFM testability is achieved without adding any extra inputs to the adder, with very small area and performance overheads, thus providing a practical solution. The proposed DFT scheme requires only 1 extra output and it is not necessary to put the circuit in a special test mode, while the earlier schemes require the addition of 2 extra inputs to set the circuit in test mode.

The adder employs a novel method for combining carries which does not require the back propagation associated with carry lookahead, and is not limited to radix-2 trees, as is the binary lookahead carry tree of R.P. Brent and H.T. Kung. The adder also utilizes a hybrid carry lookahead-carry select structure which reduces the number of carriers that need to be derived in the carry lookahead tree. This approach produces a circuit well suited for CMOS implementation because of its balanced load distribution and regular layout

S. Xing and W. W. H. Yu, "FPGA Adders: Performance Evaluation and Optimal Design," This literature also describes about, Delay models and discuss costs and operational delays of fixed-point adders on Xilinx 4000 series devices and propose timing models and optimization schemes for carry-skip and carry-select adders

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PROPOSED SYSTEM

Adders are one of the most essential components in digital building blocks, however, the performance of adders become more critical as the technology advances. The problem of addition involves algorithms in Boolean algebra and their respective circuit implementation. Algorithmically, there are linear-delay adders like ripple-carry adders (RCA), which are the most straightforward but slowest. Adders like carry-skip adders (CSKA), carry-select adders (CSEA) and carry-increment adders (CINA) are linear-based adders with optimized carry-chain and improve upon the linear chain within a ripple-carry adder. Carry-look ahead adders (CLA) have logarithmic delay and currently have evolved to parallel-prefix structures. Other schemes, like hancarlson adders, NAND/NOR adders and carry-save adders can help improve performance as well.

This gives background information on architectures of adder algorithms. In the following sections, the adders are characterized with linear gate model, which is a rough estimation of the complexity of real implementation. Although this evaluation method can be misleading for VLSI implementers, such type of estimation can provide sufficient insight to understand the design trade-offs for adder algorithms.

BLOCK DIAGRAM :

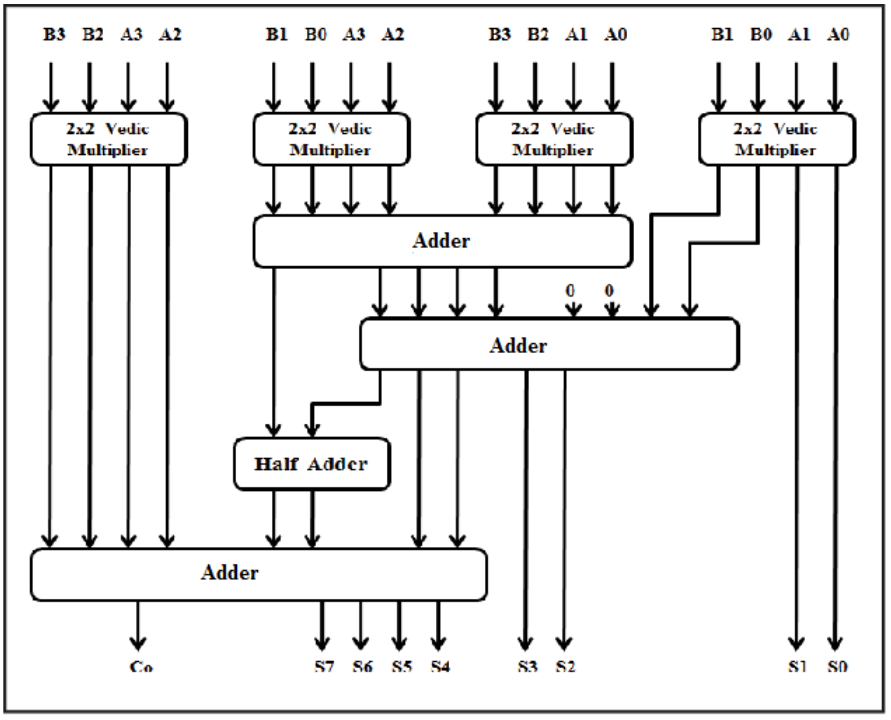


Figure.1 Block Diagram

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RESULTS

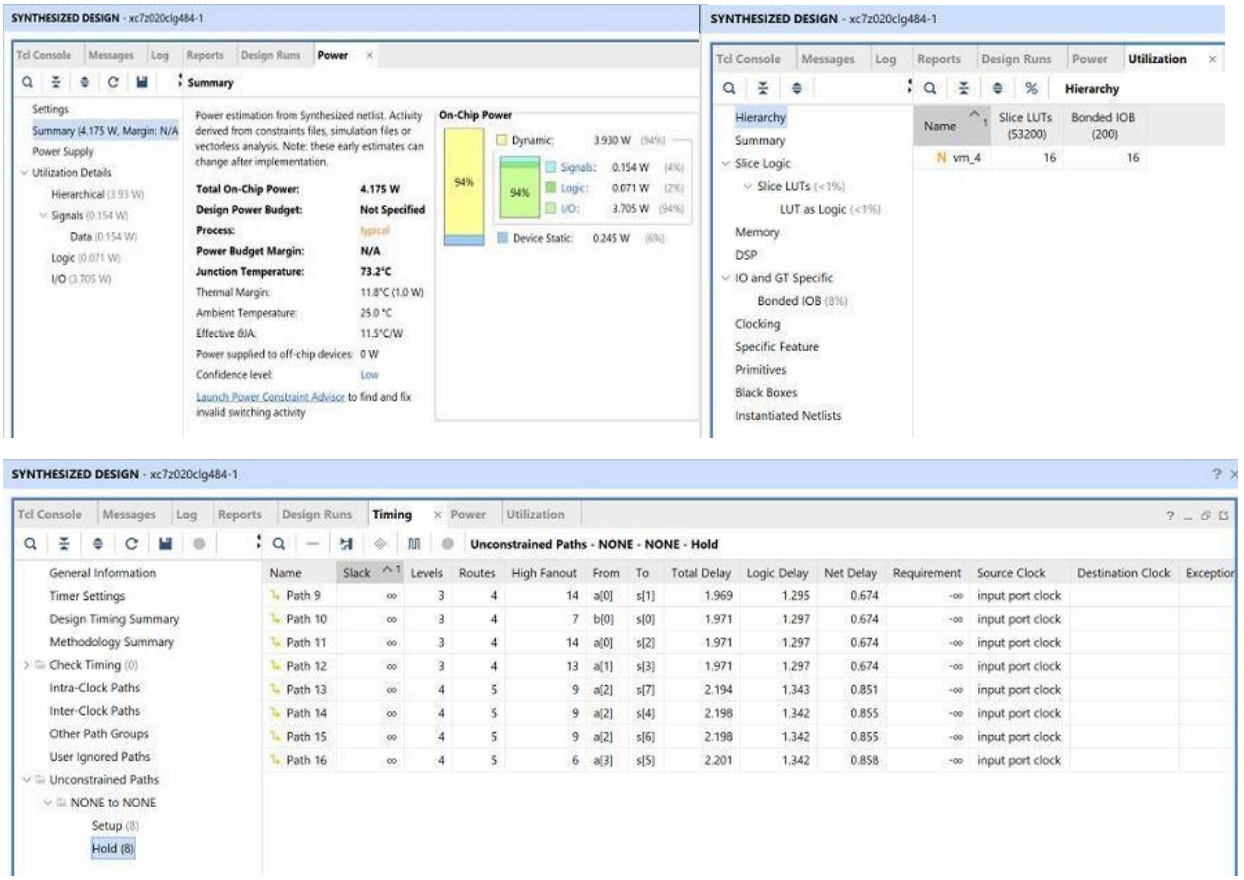


Figure. 1 Power , Area Utilization and Timing Summary

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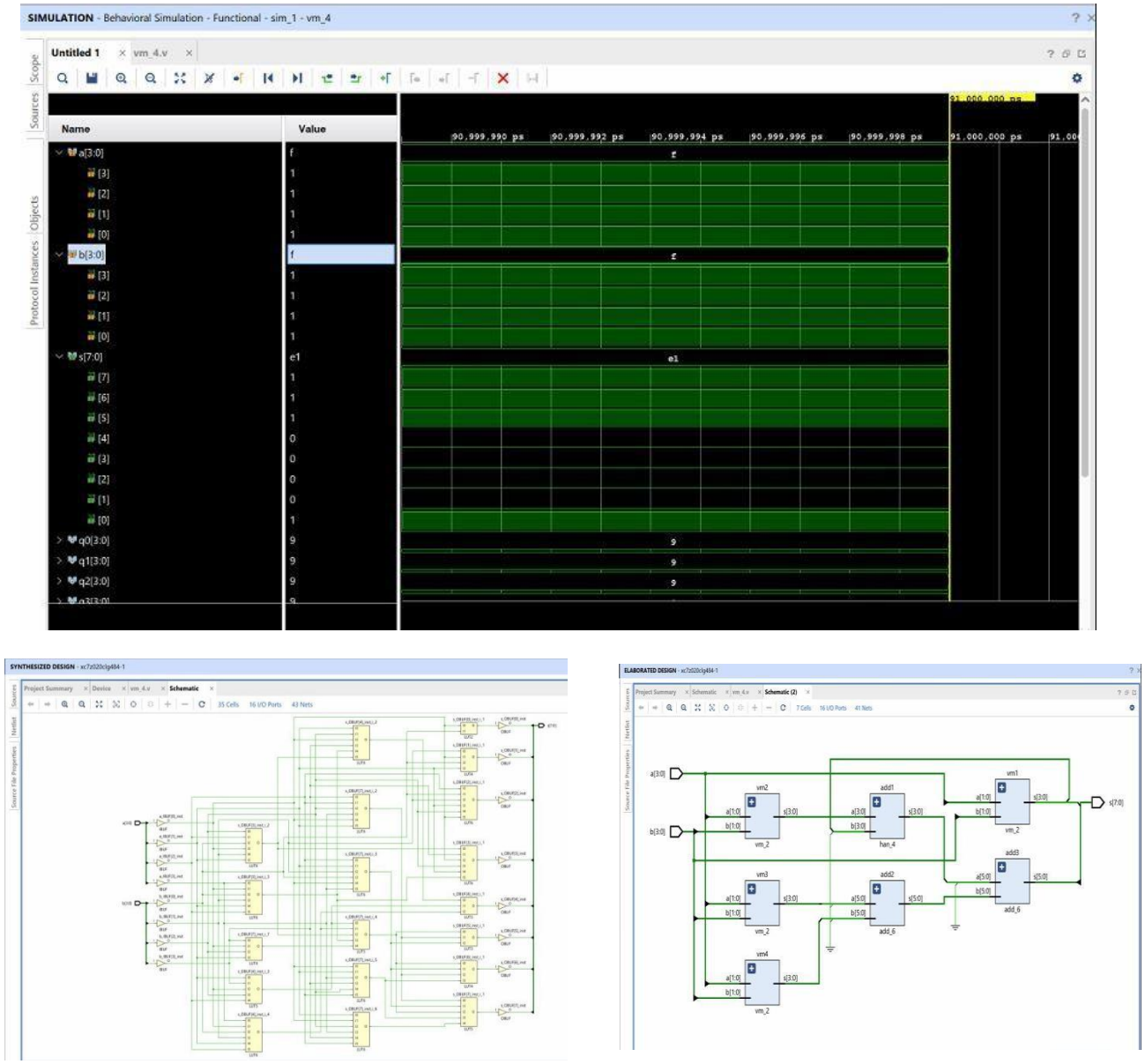


Figure. 2 RTL , Technological Schematic with Behavioral Simulation

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ADVANTAGES

- High Speed of Operation
- Less Delay
- Area Efficient
- Low Power Consumptions

APPLICATIONS

- FIR Filters
- Digital signal processors.
- Arithmetic circuits
- Image and Video Processing
- FPGA Designs

CONCLUSION

The implementation of a Vedic Multiplier using Carry Tree Adders represents a significant advancement in the field of digital signal processing and arithmetic operations. The Vedic Multiplier offers an efficient and parallel approach to multiplication. By leveraging the Carry Tree Adders, we enhance the overall performance of the multiplier in terms of speed, power efficiency, and area utilization.

One of the key advantages of the Vedic Multiplier lies in its ability to perform parallel computations, allowing for faster multiplication compared to traditional methods. This is particularly beneficial in applications where high-speed arithmetic operations are crucial, such as in signal processing and communication systems. The Carry Tree Adders further amplify this speed advantage by efficiently propagating and processing carry bits across multiple stages, minimizing critical path delays and enabling rapid calculations.

Additionally, The parallel nature of the Vedic multiplication inherently reduces the number of clock cycles required for multiplication, leading to lower power consumption per operation.

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The optimized carry propagation in the Carry Tree Adders adds to this efficiency by minimizing switching activity and dynamic power dissipation.

Moreover, The compact and modular nature of Carry Tree Adders allows for a more streamlined layout, reducing the overall silicon footprint. This is particularly important in modern integrated circuits, where efficient space utilization is critical for accommodating complex functionalities within limited chip real estate.

In conclusion, This combination of ancient mathematical principles and contemporary digital design techniques provides a promising solution for enhancing the performance of arithmetic units in various digital systems, making it a valuable contribution to the advancement of digital signal processing and computation.

FUTURE SCOPE

For Increasing number of bits in the Multiplication , Other Sutra's of the Vedic Mathematics can be applied one of which is Nikhilam navatascaramam dasatah and other Carry Select adders can be used in the Multiplier Blocks to test their Power, Area and Timing Parameters.These Vedic Multipliers can be Implemented in the Applications of Digital Signal Processing, Image and Video Processing , Design of FPGA's etc.. to Compare the Efficiencies in the form of resolution and other parameters.

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