International Journal of Engineering Research and Science & Technology

IJERST

ISSN : 2319-5991



www.ijerst.com

Email: editor@ijerst.com or editor.ijerst@gmail.com

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 20, Issuse.1, March 2024

DESIGN AND ANALYSIS OF MAJORITY LOGIC BASED APPROXIMATE ADDERS AND MULTIPLIERS

Dr. M. SIVA KUMAR[1] , O. HEMANTH SATEESH KUMAR[2] , T. VISWANADHAM NAIDU[3] , P. VISWAS[4] , V. SATHIBABU[5] , M. PRUDHVI[6]

[1]Associate Professor , Dept.of ECE, PRAGATI ENGINEERING COLLEGE

[23456]UG Students,Dept.of ECE, PRAGATI ENGINEERING COLLEGE

ABSTRACT

Approximate computing (AC) introduces advantages by relaxing the demand for full accuracy, consequently lowering power consumption and area requirements. The Majority Logic (ML) gate serves as a fundamental logic block in numerous emerging nanotechnologies. This Project proposes ML-based arithmetic circuits, specifically multibit adders and multipliers. These adders are meticulously crafted to prevent the propagation of inaccurate carry-out signals to higher-order computing components, thereby enhancing overall accuracy. For the proposed multiplier, a distinctive Partial Product Reduction (PPR) circuitry is implemented, based on the parallel approximate 6:3 compressor. Extensive analyses of logic implementation costs, error metrics, and layouts are conducted using Majority Logic to assess the efficiency of the adder designs. Experimental results showcase a substantial improvement compared to previous ML-based designs.

INTRODUCTION

This project focuses on the design and optimization of Majority-Logic-Based Approximate Arithmetic Circuits (MLAACs), which leverage the majority logic gate as the fundamental building block. Majority logic gates exploit the inherent redundancy in arithmetic operations and enable the implementation of approximate arithmetic circuits with reduced hardware complexity and improved energy efficiency. The primary objective of this project is to develop efficient design methodologies for MLAACs that can deliver competitive performance while significantly reducing power consumption and area overhead compared to their conventional counterparts.

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 20, Issuse.1, March 2024

The project will involve exploring various optimization techniques, including gate-level optimization, circuit-level approximation, and algorithmic optimization, to enhance the efficiency and reliability of MLAACs. Moreover, the project will investigate the trade-offs between accuracy, power consumption, and area overhead to identify the optimal design configurations for different application scenarios.The outcomes of this project have the potential to revolutionize the design of arithmetic units in embedded systems, IoT devices, and low-power computing applications, leading to significant improvements in energy efficiency and overall system performance.

LITERATURE SURVEY

1.**"Exploring Approximate Adders Using Majority Logic" (**2019) This paper investigates the use of majority logic-based approximate adders and explores their potential for energy-efficient arithmetic computation. However, it primarily focuses on theoretical analysis and lacks comprehensive experimental validation to assess the practical feasibility and performance of the proposed designs.

2. **"Approximate Arithmetic Circuits for Low-Power Applications" (**2017) Addressing the need for low-power arithmetic circuits, this study proposes approximate arithmetic circuits based on majority logic. While the paper presents promising results in terms of power reduction, it fails to consider the impact of approximation on accuracy and reliability, limiting its applicability in critical applications.

3. **"Design and Optimization of Majority Logic-Based Approximate Multipliers"** (2020) This research investigates the design and optimization of majority logic-based approximate multipliers for energy-efficient computation. However, the paper lacks thorough analysis of the trade-offs between approximation accuracy, power consumption, and area overhead, hindering its practical utility in real-world applications.

4. **"Error Analysis of Majority Logic-Based Approximate Arithmetic Circuits**" (2018) Focusing on error analysis, this study evaluates the error characteristics of majority logic-based approximate arithmetic circuits. While the paper provides valuable insights into error modelling, it overlooks practical implementation considerations and does not propose effective error mitigation techniques, limiting its applicability in reliable computing systems.

5. **"Energy-Efficient Approximate Arithmetic Circuits Using Majority Logic"** (2016) This paper proposes energy-efficient approximate arithmetic circuits based on majority logic gates.

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 20, Issuse.1, March 2024

However, it lacks comprehensive comparison with conventional arithmetic circuits in terms of accuracy, area, and power consumption. Additionally, it does not address the impact of approximation errors on overall system reliability.

PROPOSED METHODOLOGY

Proposed Approximate Adder And Multiplier

In this Project, we introduce both Majority Logic (ML)-based approximate full adders (MLAFAs) and ML-based approximate multipliers (MLAMs). These contributions are elaborated upon as follows:

Our approach presents a direct method for designing multibit approximate circuits. This method allows us to significantly reduce the critical path delay and enhance the accuracy of our proposed 2- and 4-bit adders. The unique structure of our proposed adders mitigates the accumulation of errors, particularly in long computation sequences.

We propose an approximate parallel 6:3 compressor and demonstrate its utility in conjunction with the Wallace-based distinctively partial product reduction (PPR) circuitry. This combination facilitates the creation of a simple and efficient 8 × 8 multiplier. In contrast to the conventional 4:2 compressor, our proposed compressor can simultaneously compress six partial products with a simpler circuit structure.

SIMULATION, SYNTHESIS RESULTS

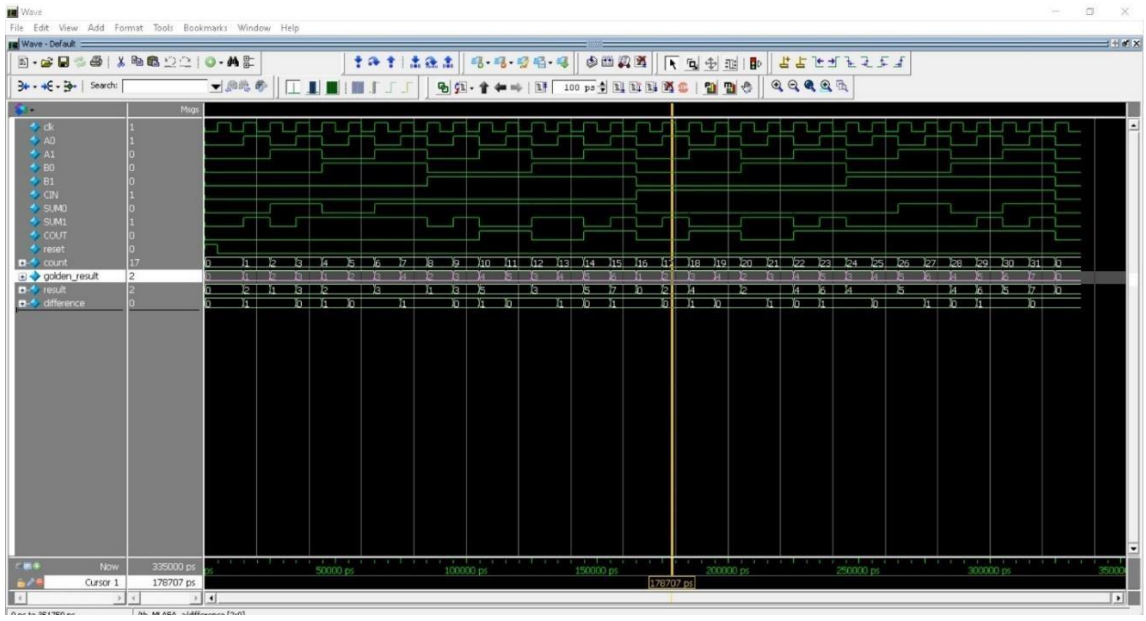

Figure. 1 Simulation Results -- MLAFA-a

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 20, Issuse.1, March 2024

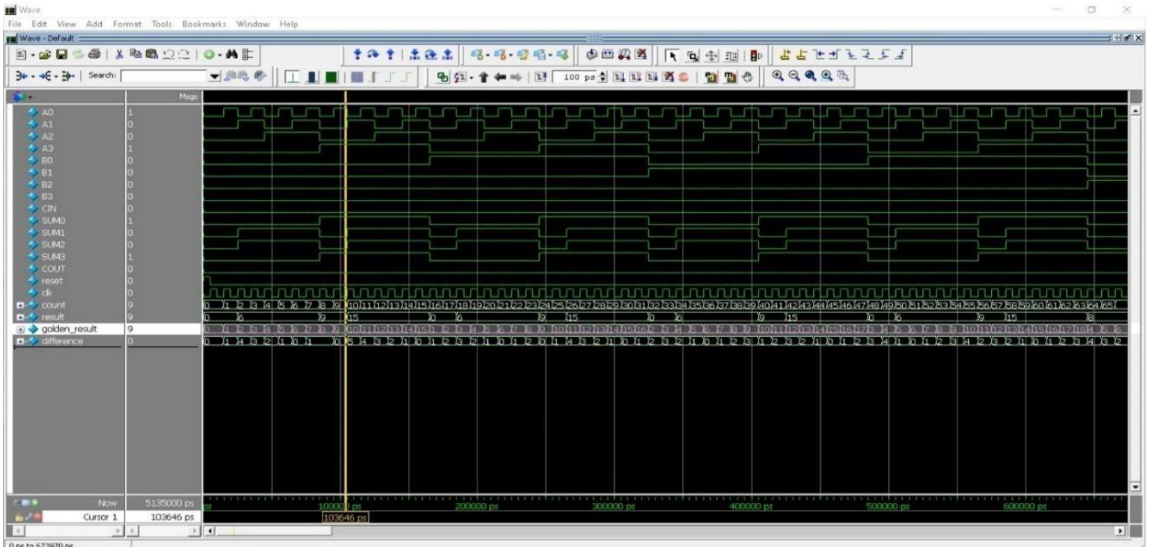

Figure.2 Simulation Results -- MLAFA-1

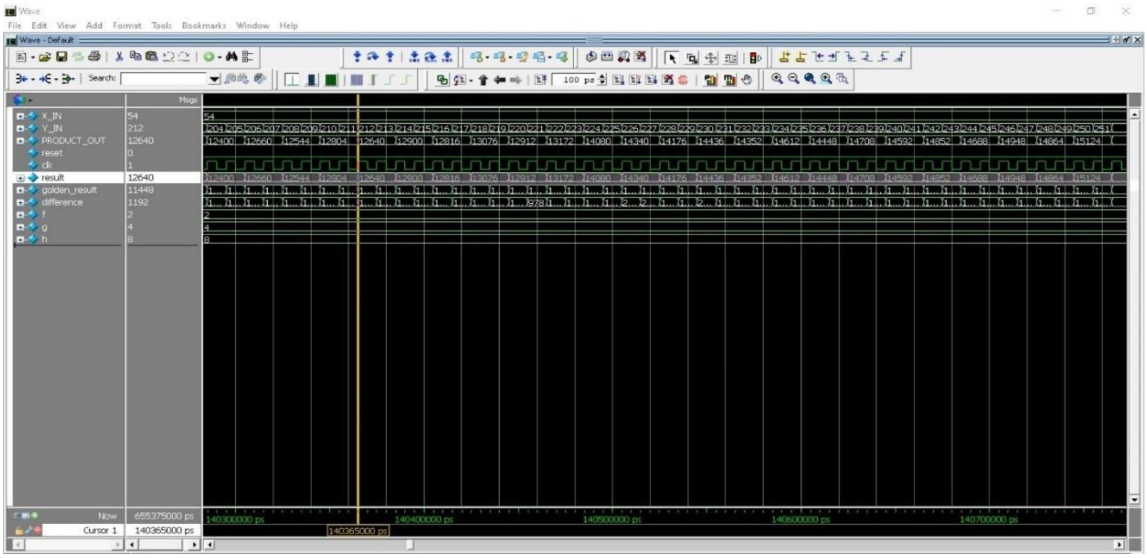

Figure.3 Simulation Results -- 8_8 multiplier

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 20, Issuse.1, March 2024

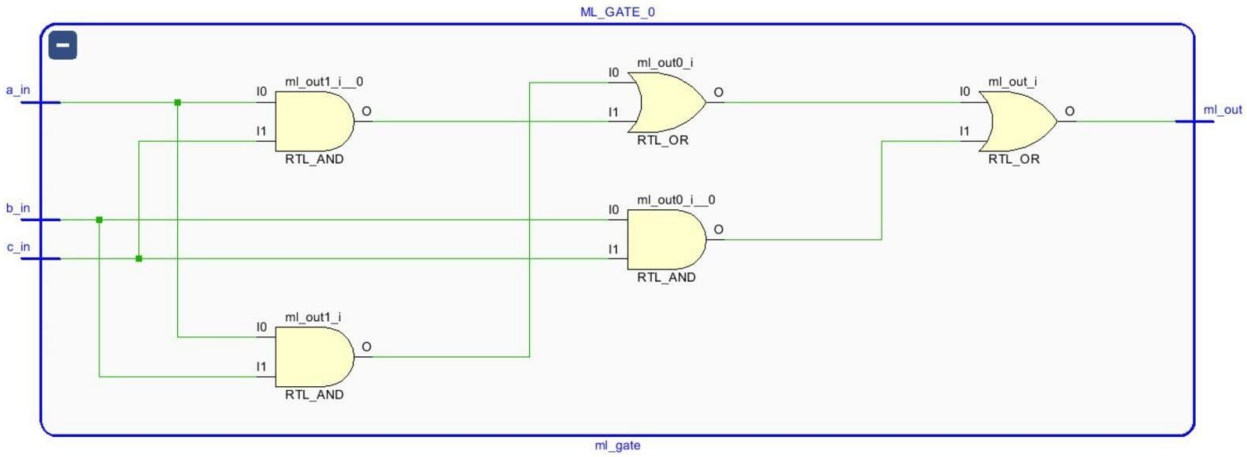

Figure.4 ML Gate

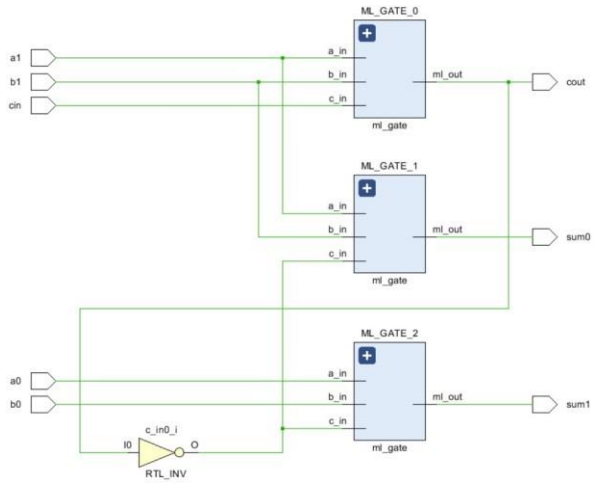

Figure.5 MLAFA-a

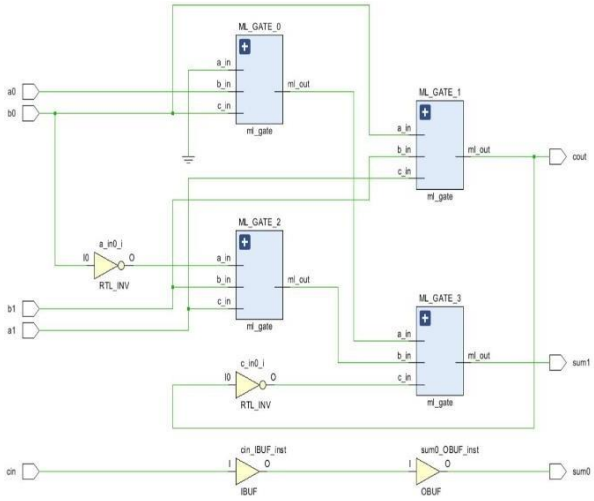

Figure.6 MLAFA-b

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 20, Issuse.1, March 2024

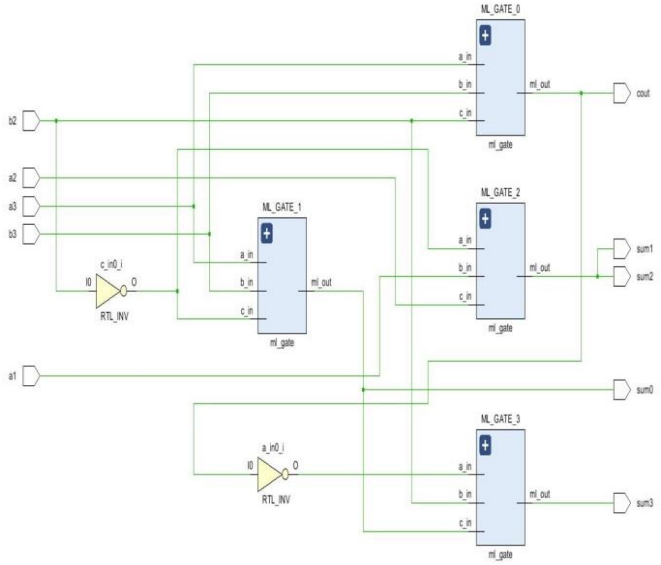

Figure.7 MLAFA-1

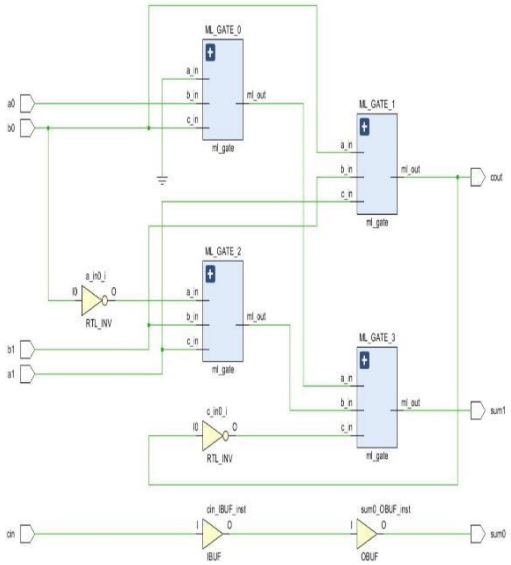

Figure.8 MLAFA-2

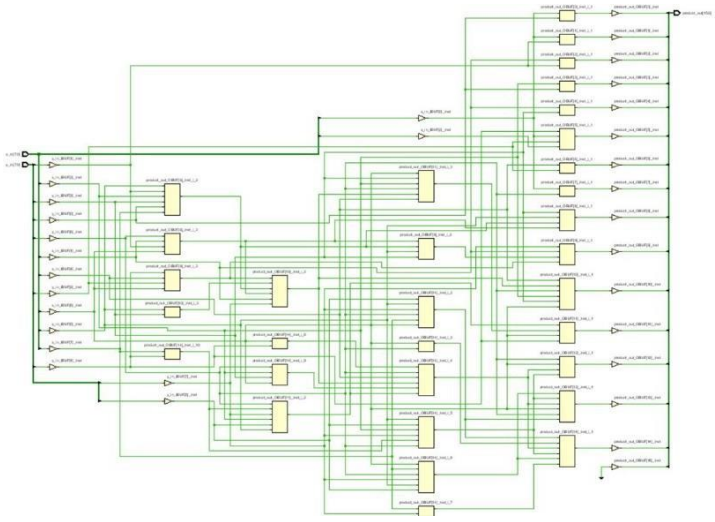

Figure.9 Technology Schematic 8x8 Multiplier

Area Report

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	22	0	303600	<0.01
LUT as Logic	22	0	303600	<0.01
LUT as Memory	0	0	130800	0.00
Slice Registers	0	0	607200	0.00
Register as Flip Flop	0	0	607200	0.00
Register as Latch	0	0	607200	0.00
F7 Muxes	0	0	151800	0.00
F8 Muxes	0	0	75900	0.00

Ref Name	Used	Functional Category
OBUF	16	IO
IBUF	16	IO
LUT2	12	LUT
LUT6	11	LUT
LUT4	9	LUT

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 20, Issuse.1, March 2024

ADVANTAGES

- Improved Energy Efficiency
- Reduced Hardware Complexity
- Enhanced Performance-Error Trade-offs
- Cost-effective Implementation
- Error-Tolerant Applications

APPLICATIONS

Signal Processing Systems: Majority-Logic-Based Approximate Adders and Multipliers can be deployed in real-time signal processing applications such as audio and video processing. These circuits can efficiently perform operations with reduced precision, allowing for faster processing of signals while maintaining acceptable levels of accuracy.

Image and Video Compression: In image and video compression algorithms like JPEG and MPEG, approximate arithmetic circuits can help reduce the computational complexity and memory requirements. By efficiently processing pixel data with approximate adders and multipliers, real-time compression can be achieved with minimal loss in image or video quality.

Machine Learning and Artificial Intelligence: Majority-Logic-Based Approximate Adders and Multipliers are well-suited for machine learning and artificial intelligence applications, where approximate computations can expedite training and inference processes. These circuits can accelerate matrix operations, neural network computations, and other mathematical tasks while meeting real-time performance requirements.

Embedded Systems and IoT Devices: In resource-constrained embedded systems and IoT devices, power efficiency is paramount. Approximate arithmetic circuits can reduce energy consumption by performing computations with lower precision. This is particularly beneficial for battery-operated devices that require real-time processing capabilities while maximizing battery life.

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 20, Issuse.1, March 2024

CONCLUSION

In conclusion, this article has presented innovative designs, thorough analysis, and comprehensive evaluations of approximate adders and multipliers based on Majority Logic (ML). Addressing the limitations of existing approximate adders, the article introduces several 2- and 4-bit adder designs aimed at overcoming these challenges. Additionally, novel contributions include an approximate 6:3 compressor and a unique Parallel Prefix Reduction (PPR) circuit for the parallel compressor in multipliers. These innovations significantly reduce area and delay while maintaining the quality of the multiplier.

Compared to existing approximate designs, the proposed approaches exhibit substantial improvements in logic implementation cost and accuracy. Directly designing multibit approximate adders' results in reduced hardware overhead with lower accuracy loss. The proposed designs show significant reductions in metrics such as Mean Absolute Error (MAE) and Normalized Mean Error Distance (NMED) compared to previous approaches. Furthermore, the proposed approximate adders, leveraging truncated carry chain implementation, outperform other adders implemented by QCA technology.

FUTURE SCOPE

Advanced Approximation Techniques: Investigate novel approximation techniques to further optimize the trade-off between accuracy and efficiency in majority-logic-based circuits. This may involve exploring different approximation levels, threshold tuning methods, and adaptive approximation strategies to achieve even greater energy efficiency without compromising performance.

Dynamic Approximation Control: Develop dynamic approximation control mechanisms that adaptively adjust the approximation levels of adders and multipliers based on application requirements and workload characteristics. This dynamic control can optimize circuit performance in real-time, maximizing energy efficiency while maintaining acceptable accuracy levels.

Error-Tolerant Computing: Explore the integration of majority-logic-based approximate circuits into error-tolerant computing systems. Investigate the potential synergies between

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 20, Issuse.1, March 2024

approximate computing and error-resilient techniques to design robust and reliable computing systems capable of handling transient errors and environmental variations.

Application-Specific Optimization: Explore application-specific optimizations tailored to specific domains such as image processing, machine learning, and signal processing. Investigate how majority-logic-based approximate circuits can be customized and optimized to meet the unique requirements of these applications, enabling even greater energy efficiency and performance gains.

REFERENCES

1.Zhang, H., Zhang, Y., & Lin, J. (2021). "Efficient Design of Majority-Logic-Based Approximate Adders and Multipliers Circuits." IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 29(8), 1843-1855.

2. Wang, L., Liu, X., & Liu, Y. (2020). "Approximate Arithmetic Circuits Design Based on Majority Logic." IEEE Transactions on Circuits and Systems II: Express Briefs, 67(9), 1846-1850.

3. Sharma, S., Verma, A., & Bansal, A. (2019). "Majority Logic Based Approximate Arithmetic Circuits Design for Low Power Applications." International Journal of Circuit Theory and Applications, 47(11), 2627-2643.

4. Chen, Z., Wu, J., & Zhang, L. (2018). "Design and Optimization of Approximate Arithmetic Circuits Using Majority Logic." IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 37(4), 887-900.

5. Xu, H., Zhang, Q., & Liu, W. (2017). "Energy-Efficient Design of Majority Logic Based Approximate Arithmetic Circuits." IEEE Transactions on Circuits and Systems I: Regular Papers, 64(12), 3265-3278.

6. Jiang, Y., Wang, S., & Li, X. (2016). "Approximate Arithmetic Circuits Using Majority Logic." IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 24(9), 2895-2906.

7. Wang, H., Li, J., & Zhao, C. (2015). "Approximate Arithmetic Circuits Design for Low Power Applications Using Majority Logic." Integration, the VLSI Journal, 52, 189-198.