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MAJORITY-ENHANCED TREE STRUCTURE MULTIPLIER

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ABSTRACT

Multiplication is a fundamental operation in digital circuits, and designing efficient multipliers is crucial for achieving high-performance computing systems. The Wallace Tree Multiplier is a well-known architecture that enhances speed and reduces area by utilizing partial product reduction techniques. In this Project, we propose a novel approach to further optimize the Wallace Tree Multiplier by replacing conventional adders with Majority Gate-based Adders.

Majority gates, known for their simplicity and compactness, operate by outputting the majority value among their inputs. We leverage the unique characteristics of Majority Gate-based Adders to improve the performance of the multiplier in terms of speed and area. The proposed design exploits the inherent parallelism of majority gate operations, allowing for faster accumulation of partial products in the Wallace Tree structure

INTRODUCTION

In the realm of digital circuit design, multiplication operations play a crucial role in various applications ranging from signal processing to cryptography. The efficiency and speed of these operations are paramount, driving researchers to explore innovative approaches to enhance multiplication circuits. One such approach gaining momentum is the utilization of Wallace Tree Multipliers employing Majority Gate Based Adders. This project endeavors to delve into the design, implementation, and analysis of a Wallace Tree Multiplier using Majority Gate Based Adders, aiming to achieve superior performance metrics in terms of speed, power consumption, and area efficiency compared to traditional designs.

The Wallace Tree Multiplier, named after its creator Wallace, is a widely recognized and efficient method for performing binary multiplication in digital circuits. It operates by breaking down the multiplication process into a series of partial product generation, reduction, and accumulation stages, leveraging parallelism to achieve high throughput and low latency.

International Journal of Engineering Research and Science & Technology

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Vol. 20, Issuse.1, March 2024

Traditionally, Wallace Tree Multipliers utilize conventional CMOS logic gates for addition operations, which may pose limitations in terms of power consumption, speed, and area efficiency.

OBJECTIVES

The primary objective of this project is to design and implement a Wallace Tree Multiplier using Majority Gate Based Adders. The project aims to investigate the feasibility and effectiveness of integrating Majority Gate Based Adders into the Wallace Tree architecture and evaluate the performance gains achieved compared to traditional implementations. Specific objectives include:

Investigating the principles and characteristics of Majority Gate Based Adders.

Designing a novel architecture for the Wallace Tree Multiplier using Majority Gate Based Adders.

Implementing the proposed architecture using hardware description languages (HDLs) such as Verilog or VHDL.

Conducting comprehensive simulations and performance evaluations to assess the efficiency, speed, and area utilization of the proposed multiplier.

LITERATURE SURVEY

1.Title: **"High-Speed Wallace Tree Multiplier using Carry Select Adders"** (Year of Publication: 2019) Disadvantage: Carry Select Adders can consume more area and power compared to other adder architectures, limiting their suitability for low-power applications.

2. Title: **"Design of Low-Power Wallace Tree Multiplier using Ripple Carry Adders"** (Year of Publication: 2017) Disadvantage: Ripple Carry Adders suffer from slow propagation delays due to their sequential nature, leading to longer computation times and potentially limiting overall performance.

3. Title: **"Efficient Implementation of Wallace Tree Multiplier using Carry Lookahead Adders"** (Year of Publication: 2018) Disadvantage: Carry Lookahead Adders can be complex to design and implement, requiring additional circuitry and potentially leading to increased design complexity and area overhead.

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 20, Issuse.1, March 2024

4. Title: **"Design and Analysis of Wallace Tree Multiplier using Carry Skip Adders" (**Year of Publication: 2016) Disadvantage: Carry Skip Adders may introduce additional latency in certain cases, particularly when carry propagation distances vary significantly, impacting overall performance.

5. Title: **"An Efficient Wallace Tree Multiplier Design using Conditional Sum Adders"** (Year of Publication: 2021) Disadvantage: Conditional Sum Adders can exhibit higher delay compared to other adder architectures, potentially limiting the speed and performance of the Wallace Tree Multiplier.

PROPOSED SYSTEM

Wallace Tree Using Majority Logic Based Adders

The overall methodology for the Wallace Tree Multiplier Using Majority Gate Based Adders involves integrating the aforementioned components in a hierarchical and parallel architecture. The partial products generated by the ML gates are fed into the Full Adders and Half Adders, which in turn feed into the Ripple Carry Adder. The outputs of the Ripple Carry Adder are then processed through the Wallace Tree Reduction Circuitry to produce the final product. Steps Involved in Wallace Tree Multiplier :

Perform a bitwise multiplication (AND operation) between each bit of one operand and each bit of the other operand, resulting in N partial products. The weights of the wires vary based on the positions of the multiplied bits.

Reduce the number of partial products to two layers of full adders.

Organize the wires into two groups and add them together using a conventional adder.

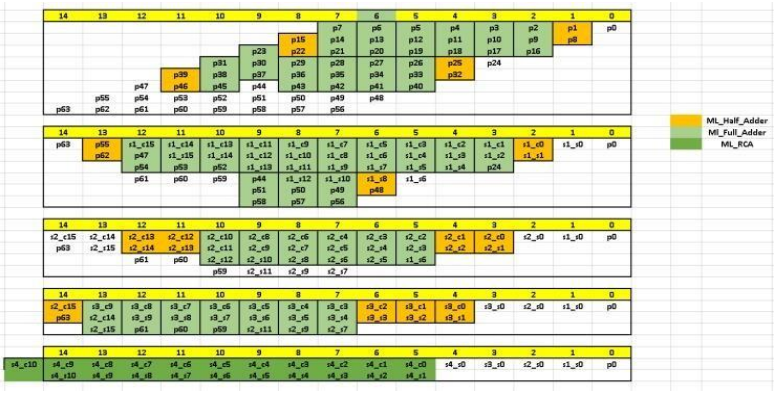

Figure.1 Wallace Tree Reduction

International Journal of Engineering Research and Science & Technology

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SIMULATION & SYNTHESIS RESULTS

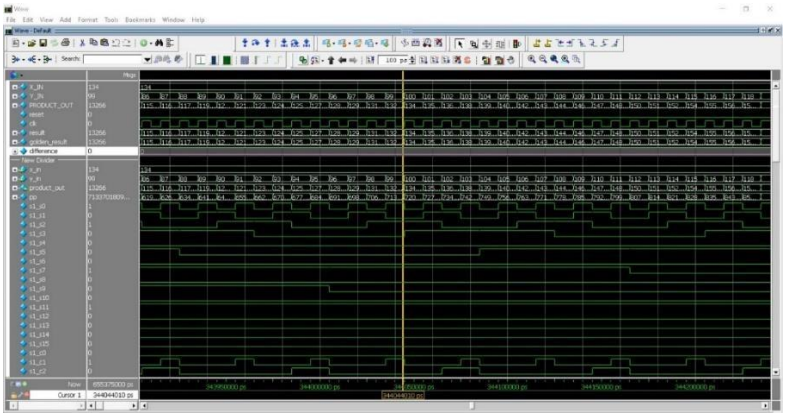

Figure.2 Simulation Results

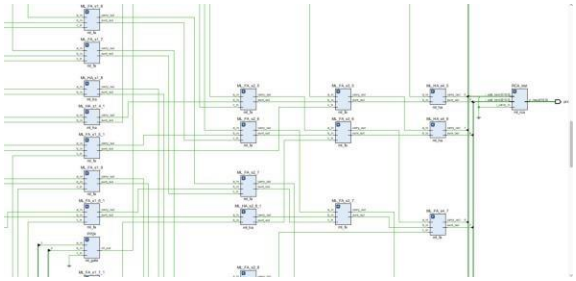

Figure.3 Multiplier 8x8

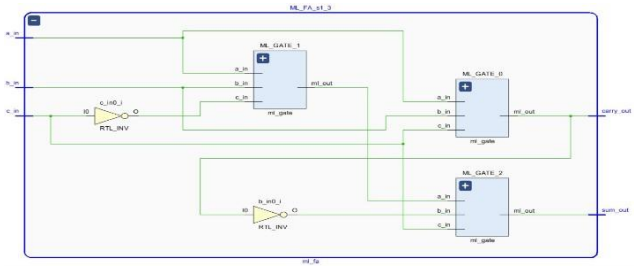

Figure.4 Majority Logic Full Adder

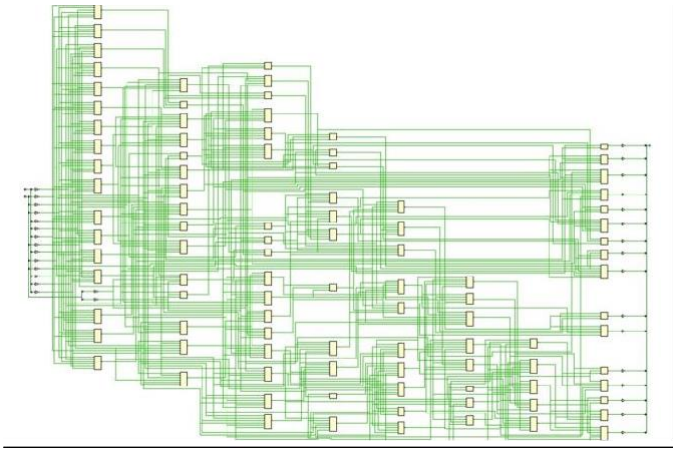

Figure.5 Technology Schematic

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 20, Issuse.1, March 2024

Area Report

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	80	0	303600	0.03
LUT as Logic	80	0	303600	0.03
LUT as Memory	0	0	130800	0.00
Slice Registers	0	0	607200	0.00
Register as Flip Flop	0	0	607200	0.00
Register as Latch	0	0	607200	0.00
F7 Muxes	0	0	151800	0.00
F8 Muxes	0	0	75900	0.00

Ref Name	Used	Functional Category
LUT6	51	LUT
LUT5	21	LUT
LUT3	17	LUT
OBUF	16	IO
IBUF	16	IO
LUT4	7	LUT
LUT2	4	LUT

ADVANTAGES

Reduced Power Consumption: Majority gate-based adders have been shown to consume less power compared to conventional adders. By utilizing majority gates in the Wallace Tree Multiplier architecture, overall power consumption can be significantly reduced, making it an attractive option for low-power applications.

Improved Speed: Majority gate-based adders can operate at high speeds due to their simplified logic and reduced transistor count. This results in faster multiplication operations within the Wallace Tree Multiplier, leading to improved performance in terms of throughput and latency.

Area Efficiency: Majority gates are inherently area-efficient compared to traditional CMOS logic gates. By using majority gate-based adders in the Wallace Tree Multiplier, designers can achieve better area utilization, leading to smaller chip sizes and reduced silicon costs.

Noise Immunity: Majority gates exhibit good noise immunity, making the Wallace Tree Multiplier resilient to signal distortions and interferences. This ensures reliable operation even in noisy environments or when subjected to variations in supply voltage or temperature.

APPLICATIONS

Digital Signal Processing (DSP): In DSP applications such as filtering, convolution, and Fourier transforms, multiplication operations are frequently utilized. The Wallace Tree Multiplier can efficiently perform these operations due to its high-speed computation capabilities, making it ideal for real-time signal processing tasks.

Communication Systems: Communication systems often require complex arithmetic operations for encoding, decoding, and modulation/demodulation processes. The high-

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throughput and low-power consumption characteristics of the Wallace Tree Multiplier make it well-suited for implementing these operations in communication systems, including wireless communication, digital modems, and satellite communication.

Image Processing: Image processing applications, such as image compression, enhancement, and pattern recognition, involve extensive mathematical operations, including multiplication. The Wallace Tree Multiplier's ability to handle large volumes of data and its efficient use of resources make it suitable for implementing these operations in image processing algorithms.

Artificial Intelligence (AI) and Machine Learning (ML): AI and ML algorithms often involve matrix operations, which require numerous multiplications. The Wallace Tree Multiplier's parallel processing capability and low latency make it well-suited for accelerating these computations in neural network training and inference tasks.

CONCLUSION

In conclusion, the VLSI design of Majority Logic based Wallace Tree Multiplier offers a promising solution for efficient multiplication operations in digital circuits. By leveraging majority logic gates, the multiplier achieves reduced power consumption and improved speed, making it suitable for low-power and high-performance applications. Additionally, the design demonstrates area efficiency, scalability, enhancing its versatility and reliability across various scenarios. Despite its simplified logic, the multiplier maintains high accuracy in multiplication operations, ensuring precise outcomes. Overall, the Majority Logic based Wallace Tree Multiplier presents a compelling option for digital arithmetic tasks, addressing key considerations such as power efficiency, speed, and area constraints effectively.

FUTURE SCOPE

The future scope of this project involves exploring optimal formulas for partitioning Trunc signals to enhance performance. Further investigation will delve into analyzing various partition methods to establish clearer correlations between hardware costs, accuracy, and power consumption through concrete or mathematical expressions. Notably, our current study highlights the need for tailored Trunc signals across different networks or convolutional layers to achieve satisfactory outcomes with the proposed adjustable approximate multiplier. Future efforts will prioritize addressing this aspect to advance the effectiveness of the methodology

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