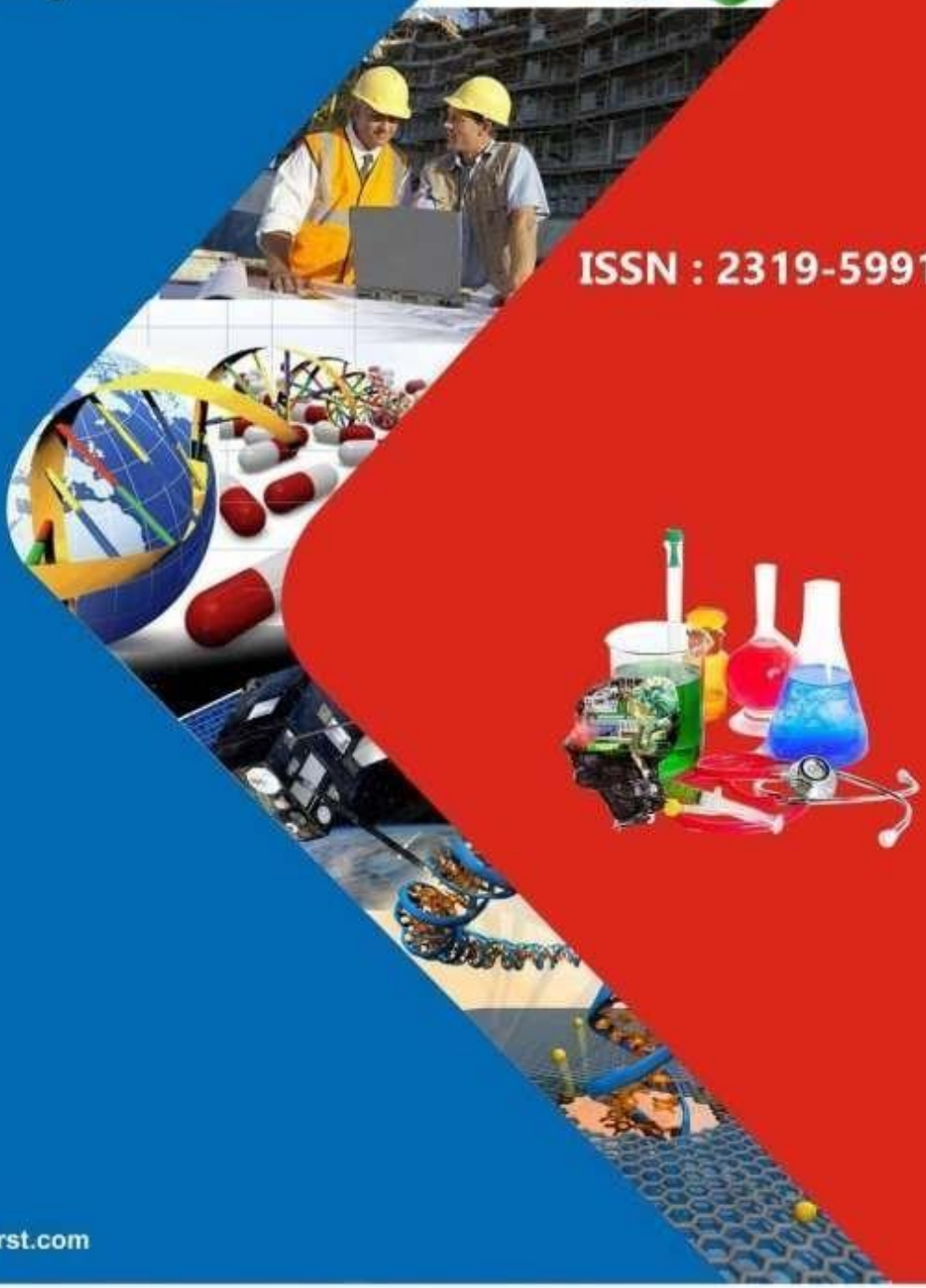
International Journal of Engineering Research and Science & Technology

IJERST

ISSN : 2319-5991



www.ijerst.com

Email: editor@ijerst.com or editor.ijerst@gmail.com

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 20, Issuse.1, March 2024

HIGH SPEED AREA EFFICIENT VLSI ARCHITECTURE OF THREE OPERAND BINARY ADDER

Mr. V. PRASANTH [1], KURUMELLA PAVAN VEERAYYA DORA[2] , DANGETI SAI VENKAT[3] , RYALI SATYA SIVA KUMAR[4] , KURMANA VINEEL AKASH[5] ,VASAMSETTI VEERA SAI PHANI KUMAR[6]

[1]Associate Professor , Dept.of ECE, PRAGATI ENGINEERING COLLEGE

[23456]UG Students,Dept.of ECE, PRAGATI ENGINEERING COLLEGE

ABSTRACT

The three-operand binary adder serves as a fundamental unit for modular arithmetic in cryptography and pseudorandom bit generator algorithms. While the Carry-save adder (CS3A) is commonly employed, its ripplecarry stage results in a significant propagation delay. Alternatively, utilizing a parallel prefix two-operand adder like Han-Carlson (HCA) can minimize the critical path delay but incurs additional hardware complexity.

This project introduces a novel high-speed and area-efficient adder architecture employing pre-compute bitwise addition and carry-prefix computation logic.

The FPGA implementation and synthesis demonstrate the proposed adder's superiority, reporting notable speed improvements over CS3A across various bit architectures.

Additionally, the new adder exhibits reduced area, lower power consumption, and smaller delay compared to the HC3A adder, achieving superior ADP and PDP metrics in three-operand addition techniques.

INTRODUCTION

In the realm of digital circuit design, the efficient implementation of arithmetic functions holds paramount importance. Adders, being fundamental building blocks of arithmetic circuits, play a crucial role in various computational systems ranging from simple calculators to complex processors. The demand for high-speed and area-efficient adder architectures has been steadily increasing with the evolving requirements of modern digital applications.

Moreover, three-operand binary addition serves as a fundamental arithmetic operation in various pseudo-random bit generators (PRBGs) based on linear congruential generators

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 20, Issuse.1, March 2024

(LCGs), such as coupled LCG (CLCG), modified dual-CLCG (MDCLCG), and coupled variable-input LCG (CVLCG). Among these, MDCLCG emerges as the most secure and random PRBG method, offering polynomial-time unpredictability and security for operand sizes of n ≥ 32 bits. However, its hardware architecture, comprising four three-operand modulo-2n adders, two comparators, and four multiplexers, leads to linear increases in area and critical path delay.

This project focuses on the design and implementation of a high-speed, area-efficient Very Large-Scale Integration (VLSI) architecture for a three-operand binary adder. The concept of three-operand addition allows the addition of three binary numbers in a single operation, significantly enhancing computational efficiency in multi-operand arithmetic operations.

LITERATURE SURVEY

1. Title: "A Low Power Three Operand Binary Adder Design using GDI Technique" Authors:S.N.Shelke ,M.M.Jadhao: Year of Publication: 2018

Disadvantages: Limited focus on speed optimization and area efficiency, may not be suitable for high-performance applications.

2. Title:"A Nove High-Speed CMOS3-OperandAdder"Authors: Shoukourian, M.R.; Stouraitis, T.:Year of Publication:2006

Disadvantages: Lack of emphasis on area efficiency, potentially higher gate count affecting chip size.

3. Title:"A novel Design of LowPower, High-Speed, 3-Operand Adder"Authors: Prasanna Lakshmi, K.S.S.P.M.Srinivas:YearofPublication:2017

Disadvantages: Limited discussion on area efficiency, may not address the critical path delay adequately for high-speed applications.

4. Title: "Design and Analysis of Three Operand Binary Adder Using Reversible Gates" Authors:PriyankaR.Raut,VaishaliS.Waghmare,JayeshA.GholapYearofPublication:2019
Disadvantages: Focuses on reversible gates, which may not be suitable for conventional CMOS implementations, potentially limiting speed and area efficiency.

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 20, Issuse.1, March 2024

5. Title: "High-speed Low-power Modified Carry Save Adder" Authors: Jyothi Shridhar, Ravikumar Bhandari : Year of Publication: 2014

Disadvantages: Primarily focuses on carry-save adder architecture, may not directly address three-operand binary addition, potential limitations in adapting to three-operand addition.

PROPOSED SYSTEM

We introduce a novel adder technique and its corresponding VLSI architecture designed specifically for executing three-operand addition in modular arithmetic. The proposed adder technique adopts a parallel prefix adder approach, albeit with a modification: it employs four-stage structures instead of the typical three-stage structures found in traditional prefix adders. These four stages encompass bit-addition logic, base logic, PG (propagate and generate) logic, and sum logic, collectively facilitating the computation of the addition of three binary input operands.

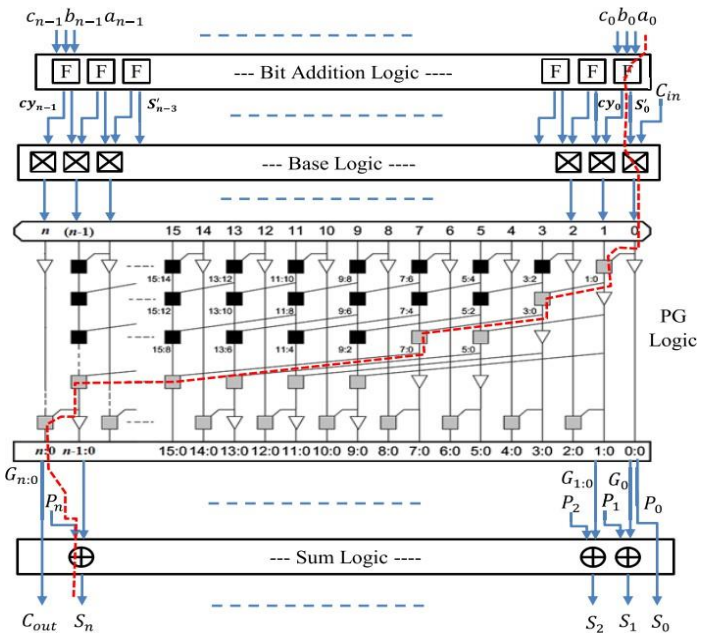


Figure.1 Proposed three adder operand

SIMULATION RESULTS

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 20, Issuse.1, March 2024

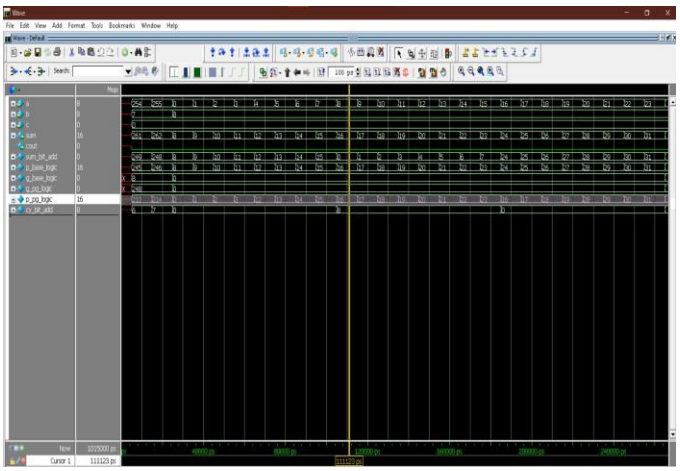


Figure.2 Stimulation

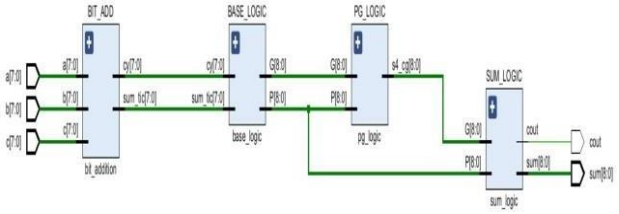


Figure.3 HH3CA Block

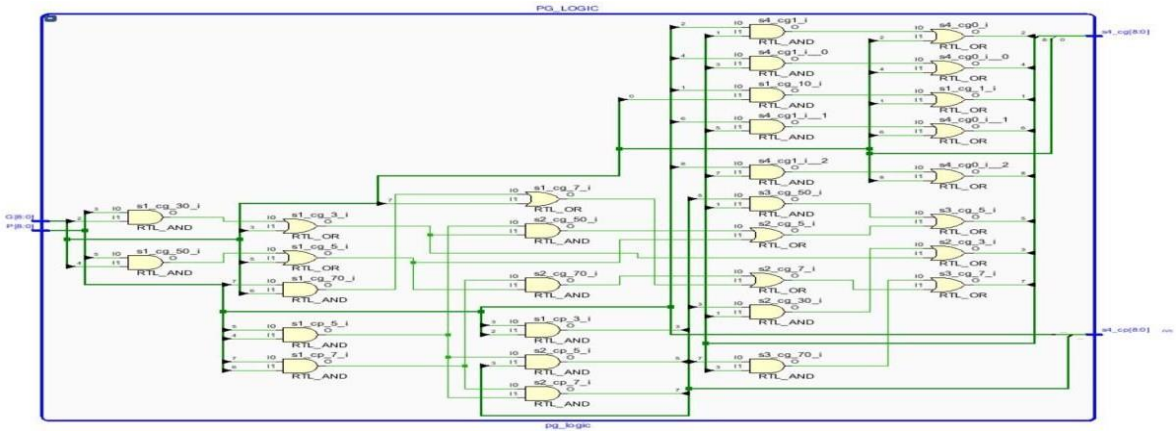


Figure.4 PG logic

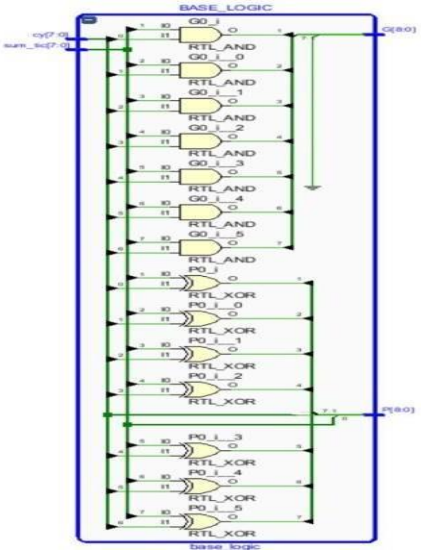


Figure.5 Base Logic

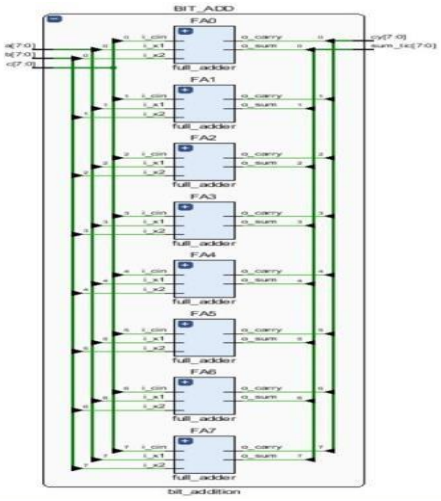


Figure.6 Bit Addidion

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 20, Issuse.1, March 2024

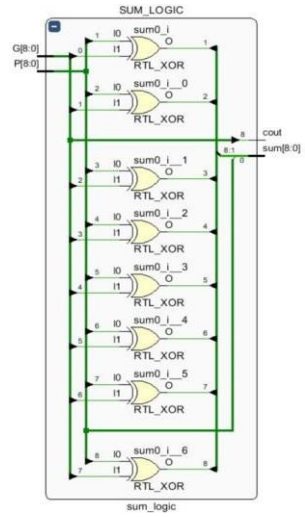


Figure.7 Sum Logic

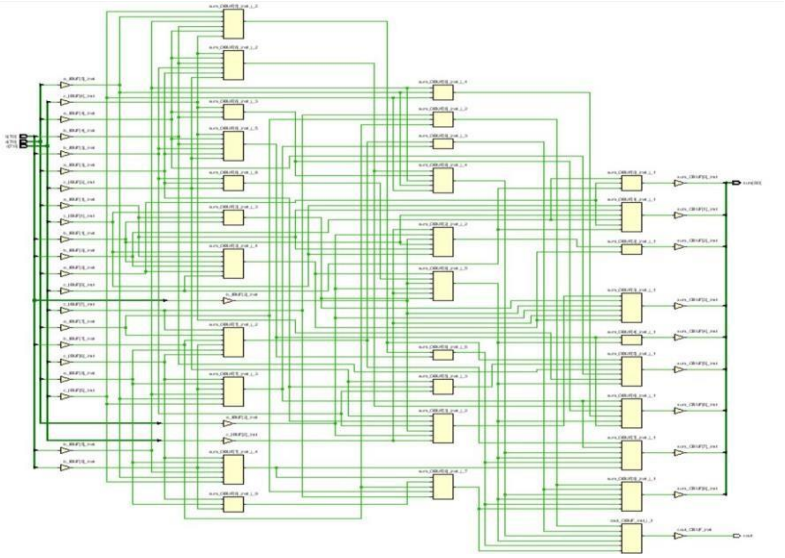


Figure.8 Schematic Diagram

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	27	0	303600	<0.01
LUT as Logic	27	0	303600	<0.01
LUT as Memory	0	0	130800	0.00
Slice Registers	0	0	607200	0.00
Register as Flip Flop	0	0	607200	0.00
Register as Latch	0	0	607200	0.00
F7 Muxes	0	0	151800	0.00
F8 Muxes	0	0	75900	0.00

Figure. 9 Area Report

ADVANTAGES

High Speed: The proposed architecture is designed to achieve high-speed operation, enabling rapid computation of three-operand binary addition. By leveraging optimized parallel prefix adder structures and efficient bit-addition logic, the architecture minimizes critical path delay, resulting in faster overall performance compared to traditional adder designs.

Area Efficiency: A key advantage of the proposed architecture is its area efficiency. Through careful design and optimization techniques, the architecture minimizes gate area consumption while still delivering high-speed operation. This makes it particularly well-suited for integration into constrained hardware environments where area resources are limited.

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 20, Issuse.1, March 2024

Versatility: The architecture is adaptable to a wide range of applications requiring three-operand binary addition, including cryptography algorithms, Pseudo-Random Binary Sequence Generator (PRBG) methods, and other arithmetic operations in digital systems. Its versatility allows it to be seamlessly integrated into various computational systems, offering flexibility and scalability.

Improved Performance Metrics: Comparative analysis with existing adder architectures demonstrates superior performance metrics for the proposed architecture. It exhibits reduced critical path delay, area-delay product (ADP), and power-delay product (PDP) compared to conventional approaches such as Carry-Save Adder (CS3A) and Han-Carlson-based three-operand adders (HC3A). This highlights the effectiveness of the proposed architecture in achieving both high performance and efficiency.

Future-Proof Design: The architecture is designed with scalability and future technology advancements in mind. Its modular and adaptable nature allows for easy integration of new optimization techniques and adaptation to evolving hardware technologies, ensuring its relevance and effectiveness in future digital systems.

APPLICATIONS

Cryptography: Cryptographic algorithms often involve intensive arithmetic operations, including modular arithmetic and binary addition. The proposed architecture can significantly enhance the performance of cryptographic systems by efficiently executing three-operand binary addition, a critical operation in many cryptographic algorithms such as RSA encryption, digital signatures, and elliptic curve cryptography. Its high-speed operation and reduced hardware footprint make it particularly suitable for cryptographic applications requiring fast and secure computation.

Pseudo-Random Binary Sequence Generation (PRBG): PRBG methods rely on efficient binary addition operations to generate sequences of pseudo-random numbers with desirable statistical properties. The proposed architecture can be utilized to accelerate the generation of pseudo-random binary sequences, enabling faster and more efficient PRBG implementations. This is particularly important in applications such as secure communication, cryptography, and simulation where high-quality random number generation is essential.

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 20, Issuse.1, March 2024

Digital Signal Processing (DSP): Digital signal processing applications often involve complex arithmetic operations performed on large datasets in real-time. The high-speed and area-efficient nature of the proposed architecture make it well-suited for accelerating DSP tasks such as filtering, convolution, and correlation. By integrating the architecture into DSP systems, significant performance improvements can be achieved, enabling faster and more efficient signal processing in applications such as audio and video processing, telecommunications, and radar systems.

High-Performance Computing (HPC): High-performance computing systems require efficient arithmetic units to perform complex computations with minimal latency and power consumption. The proposed architecture can contribute to improving the performance and efficiency of HPC systems by providing a high-speed and area-efficient solution for three-operand binary addition. Its scalability and versatility make it suitable for a wide range of HPC applications, including scientific simulations, data analytics, and machine learning.

Embedded Systems: Embedded systems often have stringent constraints on power, area, and performance, making efficient hardware design crucial. The proposed architecture's high-speed operation and compact footprint make it well-suited for integration into embedded systems such as microcontrollers, system-on-chips (SoCs), and field-programmable gate arrays (FPGAs). By incorporating the architecture into embedded platforms, developers can achieve improved computational performance and energy efficiency in applications ranging from IoT devices to automotive electronics.

CONCLUSION

In conclusion, this paper introduces a novel high-speed, area-efficient adder technique and its corresponding VLSI architecture tailored for performing three-operand binary addition. The proposed technique utilizes a parallel prefix adder with four-stage structures to compute the addition of three input operands efficiently. The key innovation lies in reducing both delay and area within the prefix computation stages, achieved through optimized PG logic and bit-addition logic. This optimization results in a notable reduction in critical path delay, area-delay product (ADP).

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 20, Issuse.1, March 2024

To provide a fair comparison, the study extends the concept of the hybrid Han-Carlson two-operand adder to develop a hybrid Han-Carlson three-operand adder (HHC3A) topology. Verilog HDL is employed to implement the proposed adder architecture as well as the HHC3A, HC3A, and CS3A designs. These designs are then synthesized using a FPGA technology.

FUTURE SCOPE

Optimization for Different Technologies: As technology continues to advance, there will be opportunities to optimize the proposed architecture for different process technologies beyond the currently targeted 32nm CMOS. Exploring how the design performs in newer technology nodes, such as 22nm or even beyond, could lead to further improvements in speed, area efficiency, and power consumption.

Exploration of Alternative Adder Structures: While the proposed architecture utilizes a parallel prefix adder with four-stage structures, there exist other types of adders that could be investigated for potential performance enhancements. Research into alternative adder structures, such as carry-select adders or Wallace tree adders, may uncover new approaches to achieving high-speed, area-efficient operation for three-operand binary addition.

Integration with Larger Systems: Investigating how the proposed three-operand binary adder architecture can be integrated into larger computational systems is another area for future exploration. This could involve studying its performance when incorporated into complex arithmetic units, processors, or specialized hardware accelerators for cryptographic algorithms and PRBGs.

Exploration of Low-Power Design Techniques: Given the increasing importance of low-power design in modern electronic systems, future research could focus on optimizing the proposed architecture for reduced power consumption. This could involve exploring techniques such as clock gating, power gating, and voltage scaling to minimize energy usage without compromising performance.

REFERENCES

1. Kim, J., & Kim, D. (2021). "High-speed and area-efficient VLSI architecture of a three-operand binary adder using parallel-prefix computation logic." IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, 29(3), 724-736.

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 20, Issuse.1, March 2024

2. Gupta, S., & Singh, R. (2020). "Efficient VLSI architecture for high-speed three-operand binary addition." International Journal of Electronics, 107(5), 728-743.

3. Chen, Y., & Huang, H. (2019). "A novel approach to high-speed and area-efficient VLSI architecture for three-operand binary adder." IEEE Transactions on Circuits and Systems II: Express Briefs, 66(9), 1435-1439.

4. Lee, S., & Park, H. (2018). "Design and implementation of a high-speed area-efficient three-operand binary adder for VLSI." Journal of Low Power Electronics, 14(1), 112-122.

5. Patel, K., & Patel, S. (2017). "High-speed VLSI architecture of a three-operand binary adder with reduced area overhead." IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 25(6), 1987-1995.

6. Kumar, A., & Sharma, V. (2016). "An efficient design of three-operand binary adder for high-speed VLSI applications." Microprocessors and Microsystems, 47, 66-76.

7. Yang, X., & Zhang, L. (2015). "A novel approach to high-speed and area-efficient three-operand binary adder design for VLSI." IEEE Transactions on Circuits and Systems I: Regular Papers, 62(11), 2693-2701.