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Research

System-Level Design and Behavioural Implementation of a Second–Order CT Sigma-Delta Modulator

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***Abstract*—This paper presents the system-level design and behavioural implementation of a second-order continuous-time (CT)sigma-delta modulator for high-resolution, low-frequency sensing applications. The modulator architecture is synthesized using the MATLAB Delta-Sigma Toolbox and implemented behaviorally in Cadence Virtuoso using Verilog-A models. A cascade of integrators feed-forward (CIFF) architecture with a 1-bit quantizer and an oversampling ratio (OSR) of 12 is employed to achieve high resolution while maintaining stability. The discrete-time noise transfer function (NTF) is transformed to its continuous-time equivalent using the impulse-invariant transformation with an NRZ feedback DAC pulse. Simulation results demonstrate practical second-order noise shaping. For a 900 mV, 1 Hz sinusoidal input, the modulator achieves an SNR of 86dB, corresponding to an effective number of bits (ENOB) of 14 bits. The influence of the integrator's finite DC gain and limited gain-bandwidth product (GBW) on performance is also evaluated. The results validate the proposed modulator architecture for precision low-bandwidth sensing front-end applications.**

***Keywords*—Sigma Delta Modulator(SDM), Continuous Time Modulator, Noise shaping, CIFF Architecture, High Resolution Data conversion, Low Frequency Sensing.**

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I. INTRODUCTION

The Sigma-Delta architecture is a recent design that offers exceptional precision but is the slowest among popular architectures, making it particularly suitable for low-speed, high-resolution applications such as temperature sensing.ADCs are needed to digitize analog temperature signals and measure temperature. Temperature changes slowly, hence a low-bandwidth ADC is acceptable. The ADC must be high-resolution and suited for low-frequency applications. Resolution is the smallest analog input change an ADC can detect and convert to an output. Resolution is usually the number of bits the ADC outputs. The number of bits an ADC uses to convert an analog input to a digital output is called its resolution. Digital output accuracy requires higher resolution. ADC speed is restricted by resolution since more data must be transformed.

Among various ADC architectures, sigma-delta modulators are particularly suitable for such applications due to their oversampling and noise-shaping capabilities, which enable high precision while relaxing stringent analog circuit requirements. A continuous-time (CT) sigma-delta architecture provides additional benefits, such as inherent anti-aliasing and improved power efficiency, compared to discrete-time implementations. However, practical implementations are affected by non-idealities, including finite integrator gain and a limited gain-bandwidth product (GBW), which can degrade performance and stability.

This work presents the system-level design and behavioural implementation of a second-order CT sigma-delta modulator using CIFF architecture. The impact of key non-idealities is analysed to determine minimum design requirements for maintaining high-resolution performance.

II. LITERATURE SURVEY

A low-voltage TSMC 180nm temperature sensor with a sigma-delta modulator is described in this paper[7]. The sensor operates from -20°C to +125°C with a 1V supplied voltage. A Sigma-Delta modulator processes bandgap current reference circuit currents

proportional to absolute temperature to provide a digital output. A Sigma-Delta modulator with few components can be implemented using currents as inputs. Simulated power consumption is 120 μW, with a duty-cycle variation of 0.532% per Celsius and a low nonlinearity of 0.31% for this architecture. The sensor's small size (285 μm × 190 μm) and efficiency make it suitable for low-power, digital-output analysis applications, including wireless sensor networks and environmental monitoring.

The paper [5] designs and simulates a 24-bit sigma-delta ADC in Simulink using oversampling and noise shaping. System modulator coefficients are calculated using MATLAB. During design, clock jitter, operational amplifier noise, and KT/C noise are assessed and mitigated. A feed-forward, single-loop, one-bit quantization modulator with a 128x oversampling ratio and sixth-order is chosen for its simplicity, high signal-to-noise ratio, and robustness to non-ideal parameters. This architecture is simple, has a high signal-to-noise ratio, and is immune to clock jitter, operational amplifier noise, and KT/C noise. Non-ideal variables in the design process allow for thorough noise and distortion mitigation. Output power spectral density modeling and ENOB assessment verify that the system meets performance requirements. This architecture has a 126dB signal-to-noise ratio, making it suited for medical and industrial applications. The study emphasizes the need to balance performance, resolution, and non-ideal aspects in the design of high-resolution sigma-delta ADCs.

MATLAB simulation results are presented for Sigma Delta ADC modulators, which were compared, analysed, and simulated in the study [6]. The study compares Sigma-Delta ADC ordering across ideal-model, system-level, and behavioural-model simulations in Simulink and SimSides. The simulation results show that the simulation model affects the SNR and ENOB of ADC modulators. The Simsides model, which accounts for parasitic elements, noise, and other issues, has lower SNR and ENOB than ideal or system-level models under the same conditions. This suggests that Simsides' model simulations better represent ADC performance under challenging situations. A comparative table presents the simulation results for numerous Sigma-Delta ADC modulators, highlighting performance differences, including SNR. and ENOB. The comparison table speeds the evaluation of ADC modulators of different orders across simulation models. The table shows that increasing the modulator order increases SNR and ENOB, thereby enhancing ADC performance. The research shows that adopting the appropriate simulation model is crucial for accurately assessing the performance of Sigma-Delta ADC modulators. Researchers can better understand ADC behaviour in practical applications by accounting for parasitic components, noise, and simulation conditions.

For LoRa applications, this study[21] designs and implements Sigma-Delta ADCs in 65nm digital CMOS technology. This project aims to develop a low-power, compact single-chip sensor-transceiver system. Sigma-delta ADCs were modeled and simulated in MATLAB to account for design flaws. Sigma-Delta ADCs were chosen for their digital-domain architecture, resolution-bandwidth product, and linearity. Four topologies, first-order and second-order continuous-time modulators, and discrete-time modulators are designed and implemented in this study. Power, ENOB, and SNDR of the four topologies are measured and documented. The power distribution study shows that the design's ring oscillator consumes the most power among modulator blocks, emphasizing the need for power minimization. Due to the lack of sampling circuitry, continuous-time topologies consume less power than discrete-time modulators. The first-order CT Sigma-Delta ADC is the best design, achieving an ENOB of 7.1426 bits, an SNR of 44.7583 dB, and a power consumption of 1.44 mW at an input amplitude of 5 mV, delivering high performance with low power consumption and meeting LoRa-compliant target parameters. This study improves LoRa-compliant ADC performance while meeting power consumption goals.

The paper [12] explores an Inverter-Based Continuous-Time Sigma-Delta ADC with Latency-Free DAC calibration. To reduce DAC nonlinearity without latency, this technique uses a redesigned quantizer for background calibration. A proportional-integrating element can correct loop delay in a CTSD ADC's loop filter, improving signal swing and performance. DC power economy and performance are enhanced by the loop filter's two-stage inverter-based amplifiers. Noise performance, maximum stable amplitude (MSA), complexity, and power consumption must be balanced when adopting the CTSD ADC architecture, according to the research. Using a fourth-order architecture with a 4-bit quantizer and an OBG of 2.2, this approach provides sufficient compromise. Results show a 70 dB dynamic range, 67.3 dB peak SNDR, and 68.1 dB peak SNR, making this design suitable for demanding wireless communication systems and beyond. This emphasizes the importance of calibrating techniques to reduce nonidealities and improve ADC performance.

III. SIGMA-DELTA MODULATOR AND FORMULATION

Sigma-Delta ADCs convert analog signals to digital bit streams. Sigma-delta ADCs use modulators and decimators. A Sigma-Delta ADC is shown below in Fig.1

Sigma-delta ADCs comprise a digital-to-analog converter (DAC), an integrator, a latching comparator or quantizer, and a digital filter [6]. A feedback loop compels the DAC output, an approximation of the input, to align with the sampled analog input. An integrator computes the disparity between the actual input and the desired DAC output.

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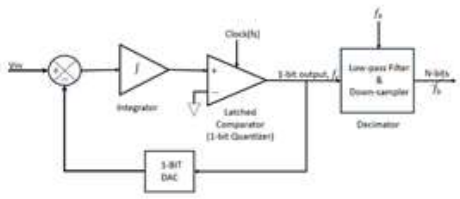

Fig. 1. Architecture of Sigma-Delta ADC

To reverse modulator operation, the latched comparator output becomes positive, prompting the DAC to transmit a positive reference signal to the error block input if the integrator output is positive. When the integrator output is negative, the latching comparator output is also negative, resulting in the DAC providing a negative reference voltage. The latch comparator produces a 1-bit output at high frequency by utilizing the integrator's output. The modulator produces HIGH (1) and LOW (0) outputs in varying ratios contingent upon the input value. As a result of design feedback, the averages of the input signal and the latched comparator output are consistent. A decimator consists of a low-pass filter (LPF) and a down-sampler. The decimator acquires the digital output from the latched comparator. The digital decimator converts the modulator's output into a low-frequency digital stream. The decimator produces data at twice the input rate. The Nyquist frequency is double the frequency of the input signal. The following are ADC performance metrics.

A. *Signal to Noise Ratio (SNR):*

The ratio of the input signal's power to the noise signal's power inside the signal band, eliminating harmonic power and considering only the modulator's linear performance. The signal-to-noise ratio equation is

$$SNR = 10log\frac{P_{signal}}{P_{noise(inband)}} \quad (1)$$

where $Psignal$ is the input signal's power and $Pnoise(inband)$ is the noise signal's power within the signal band.

B. *Signal to Noise Distortion Ratio (SNDR):*

The SNDR is the input signal's root-mean-square value relative to the root-sum-square of the harmonics and noise, minus the DC component. The SNDR includes all noise and distortion sources, making it a good predictor of the ADC's dynamic performance in dB.

C. *Dynamic Range (DR):*

The ratio between an ADC's highest and lowest signals is its dynamic range, usually in dB. DR specifications can help topologies that can't meet ADC's maximum SNR at full-scale input.

$$DR = 20log\frac{P_{max}}{P_{min}}dB \quad (2)$$

In the above equation, $Pmax$ is the most significant signal power, and $Pmin$ is the minimum signal power.

D. *Effective Number of Bits (ENOB):*

Effective Number of Bits is the number of bits a perfect Nyquist data converter needs to match a sigma-delta ADC's dynamic range.

$$ENOB = \frac{SNR-0.76}{6.02}bits \quad (3)$$

IV. Quantization Noise and Oversampling

An oversampled ADC is constructed if an ADC operates more quickly than twice the signal bandwidth (fb). ΣΔ ADCs are a type of oversampled ADC.

The oversampling ratio (OSR) requires that the sampling rate (fs) be greater than twice the input signal frequency, i.e., Nyquist's frequency.

$$OSR = \frac{f_s}{2f_b} \quad (4)$$

Oversampling ADCs offer a significant advantage over Nyquist-rate converters, since the sampling frequency is much higher than the signal bandwidth, allowing spectral replicas to be widely separated and relaxing the requirement on the anti-aliasing filter. In addition, oversampling reduces in-band quantization noise, thereby improving the converter's effective resolution. For an N-bit uniform quantizer, the step size is $\Delta V_{Full-scale}$ is, where $scale$ is the input signal full scale value. Assuming error is uniformly distributed across $-\frac{\Delta}{2}\ to + \frac{\Delta}{2}$. Then noise power (PQ).

$$P_Q = \frac{1}{\delta}\int_{-\frac{\delta}{2}}^{\frac{\delta}{2}} Q^2 dQ = \frac{\delta^2}{12} \quad (5)$$

We usually assume quantization noise power to be white noise for analysis purposes [10] and evenly distributed between- $fs2$ and $+\frac{f_s}{2}$. In reality, quantization noise is non-white because it depends on the source signal. The following equation gives the quantization noise power.

$$P_{Q,inband} = \int_{-f_b}^{f_b}\frac{P_Q}{f_s}df = \frac{P_Q}{\frac{f_s}{2f_b}} = \frac{P_Q}{K} \quad (6)$$

where $K = \frac{f_s}{2f_b}$ and stands for the oversampling ratio (OSR). From equation (6), it can be observed that the strength of the noise frequency decreases as the sampling rate increases. A digital filter can be used to minimize quantization noise that falls outside the signal frequency. As quantization noise reduces, SNR and resolution rise simultaneously.

A. *Noise Shaping in Sigma-Delta ADC*

In addition to oversampling, noise shaping is a key feature of the sigma-delta ADC. The integrator in a delta-sigma architecture [5] pushes quantization noise to high frequencies, thereby improving the SNR. The linearized 1st-order SDM model is shown in Figure 2.

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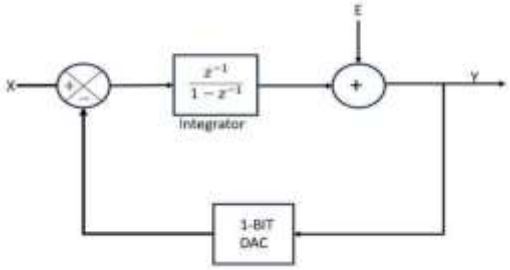

Fig. 2. First Order SDM

The input and output can be expressed as X and Y, $\frac{Z^{-1}}{1-Z^{-1}}$ block represents an integrator. E represents error due to quantization.

$$Y = Z^{-1}X + (1 - Z^{-1})E$$

$$STF = \frac{Y}{X} = Z^{-1}$$

$$NTF = \frac{Y}{E} = 1 - Z^{-1}$$

Where NTF = Noise signal transfer function for 1st Order DSM, STF=Signal Transfer Function, we can infer that noise will be attenuated at low frequencies and pushed from the signal band due to the high-pass filter action of the $1 - Z^{-1}$ block. This pushing of noise is known as noise-shaping. The noise power within the signal band after noise shaping is represented by equation (10).

$$P_{Q,inband} = \int_{-f_b}^{f_b} \frac{P_Q}{f_s} |1 - exp\left(-\frac{j2\pi f}{f_s}\right)|^2 df$$

$$\cong \frac{P_Q}{K^3}\frac{\pi^2}{3} \quad (10)$$

By comparing equations (10) and (6), we can infer that in-band quantization noise power attenuation will be greater with noise shaping. For a 1st-order SDM, the signal-to-noise ratio (SNR) is given by equation (11).

$$SNR = 6.02N + 1.76 + 30\,log(K) - 10\log\left(\frac{\pi^2}{3}\right) \quad (11)$$

Where K stands for the oversampling ratio(OSR) used, and N stands for the quantizer type used. According to equation (11), for a doubling of the sampling rate, the SNR will increase by 9dB and, consequently, the ADC resolution will increase.

B. Second Order SDM's

A higher-order sigma-delta modulator is designed using cascaded integrator stages. There will be significant attenuation of in-band noise power due to cascaded multiple integrator stages within the modulator. These high-order modulator designs will improve signal-to-noise ratio and resolution.

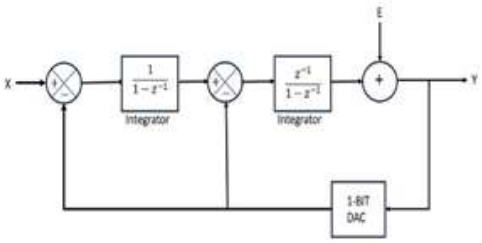

Fig. 3. 2nd-order sigma-delta modulator linearized model

Figure 3 shows a 2nd-order SDM model. In second-order SDM, two integrator stages are cascaded. The transfer function of a 2nd-order SDM from the above model can be derived as follows.

$$Y = Z^{-1}X + (1 - Z^{-1})^2 E \quad (12)$$

(7)

$$STF = \frac{Y}{X} = Z^{-1} \quad (13)$$

(8)

$$NTF = \frac{Y}{E} = (1 - Z^{-1})^2 \quad (14)$$

(9)

where NTF denotes the Transfer Function of the noise signal, and the Transfer Function of the signal is denoted by STF. The figure below shows the Magnitude Response of the 1st and 2nd order SDM's Noise Transfer Function(NTF).

The 2nd-order SDM provides more in-band quantization noise suppression, resulting in better noise shaping than the first-order SDM, as shown in Figure 3 above. The signal-to-noise ratio (SNR) of the 2nd-order SDM is derived in equation (15).

$$SNR = 6.02N + 1.76 + 50\,log(K) - 10log\left(\frac{\pi^4}{5}\right) \quad (15)$$

where K stands for the oversampling ratio(OSR) used, and N stands for the quantizer type used. According to equation (13), for a doubling of the sampling rate, the SNR increases by 15dB, and the ENOB increases by 2.5 bits. In the 2nd-order SDM, two integrator stages are cascaded. Likewise, in a 3rd-order SDM, three integrator stages are cascaded. An Lth SDM can attain a maximum SNR as shown by Equation (16).

$$SNR = 6.02N + 1.76 + 10(2L + 1)\,log(M) - 10log\left(\frac{\pi^{2L}}{2L+1}\right) \quad (16)$$

While higher-order modulators offer improved noise suppression, increasing the loop filter order may introduce stability concerns. For single-bit quantizers, stability is commonly ensured by limiting the out-of-band gain(OBG)according to Lee's criteria

V. System-Level Design Of SDM

To accurately sense temperature, a sigma-delta ADC with high-resolution output is required. So, the Sigma Delta modulator specifications for temperature sensing are a resolution (ENOB) of 12-

14 bits and a Signal-to-Noise Ratio (SNR) greater than 80dB.

A. Architecture Selection:

Suitable architecture must be selected to meet the design specifications. The loop filter order, oversampling ratio, N-bit quantizer, out-of-band gain, and the transfer function of the noise signal are the main parameters in the SDM architecture.

The modulator's architecture, along with variables such as the modulator (L) order, the noise-signal transfer function, Oversampling Ratio (OSR), & N-bit quantizer, is chosen first in the design process. Significantly higher SNR is achieved with higher-order modulators, but this comes at the cost of increased circuit complexity and decreased stability. To maintain system stability and limit complexity, a 2nd-order loop filter is chosen.

Since the single-bit quantizer is inherently linear and does not display mismatch during the quantization process, the multibit quantizer, however, exhibits irregularity in quantization steps and is more difficult and power-consuming. For the sake of linearity, a single-bit quantizer is chosen for our architecture. To achieve the required ENOB of 12-14 bits, an OSR of 128 was selected.

Lee's criteria state that the Out-of-band Gain (OBG) must be approximately 1.5 for a single-bit quantizer and between 1.5 and 3.5 for a multibit quantizer to assure stability. The most popular architectures for implementing a Sigma Delta ADC are Integrators cascaded in feedforward (CIFF) and Integrators cascaded in feedback (CIFB). Because a large number of DACs must be used in the feedback path, increasing the power demand of the digital feedback channel, Cascade of Integrators in Feedback (CIFB) is typically not the most power-efficient solution for low-power Sigma Delta ADC design. The large signal swing at the integrator stage's output is also a severe issue in CIFB architecture. At the same time, the CIFF architecture overcomes the disadvantages of the 30 CIFB architecture. Because of its minimal output swing and low power consumption, the Integrators cascaded in Feed-Forward (CIFF) design choice is made [13]. Table III lists the parameters chosen for the CT sigma-delta modulator design.

TABLE I. SYSTEM-LEVEL TEM-LEVELTEM PARAMETERS FOR THE CT-SDM DESIGN

Parameter	***Value***
Order	2nd Order
Architecture	CIFF
Oversampling Ratio (OSR)	128
Quantizer	1-bit Quantizer

The figure(4) below shows the CIFF architecture implemented in the 2nd-order SDM design.

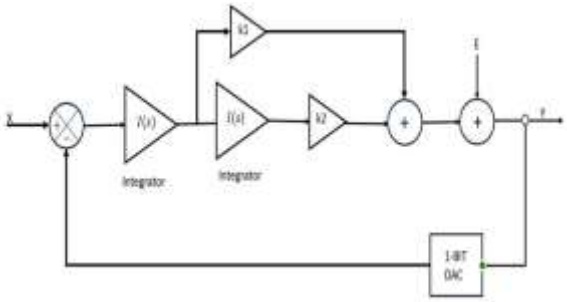

Fig. 4. CIFF architecture of the CTSDM

B. Design Of Modulator:

Equation (17) shows the relationship between NTF and loop transfer function $L[Z]$.

$$L = \frac{1}{NTF} - 1 \tag{17}$$

After the transfer function of the loop filter for the DT-SDM is generated, the corresponding loop transfer function for the CTSDM is estimated. The loop filter for the CT modulator is calculated from the corresponding DT loop filter using the impulse-invariant transformation.

Estimation of CT loop filter: The NTF of a 2nd-order discrete-time SDM with an OBG of 1.5 and an OSR of 128 is calculated using the Sigma-Delta tools in MATLAB.

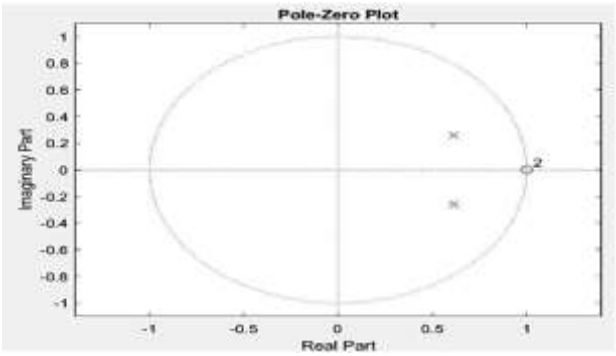

Fig. 5. Location of poles for NTF with OBG=1.5

The NTF obtained is,

$$NTF = \frac{Z^2 - 2Z + 1}{Z^2 - 1.225Z + .4415} \tag{18}$$

Figure 6 represents the 2nd-order SDM's NTF Response for OBG =1.5 and OBG =4.

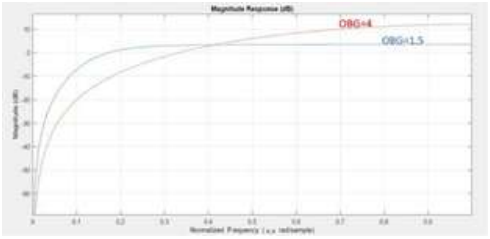

Fig. 6. 2nd order SDM's NTF Response for OBG =1.5 and OBG =4

DT loop filter L(Z) from NTF is obtained as, as, $L(Z) = \frac{1}{NTF(Z)} - 1$

$$L(Z) = \frac{0.775Z^{-1}(1-0.7206^{-1})}{(1-Z^{-1})^2} \quad (19)$$

The equivalent Continuous-Time loop filter($L(S)$) is estimated for Integrators cascaded in feedforward (CIFF) construction from the DT loop filter ($L(Z)$), based on the impulse-invariance transformation (IIT) method. The estimated CT loop filter is,

$$L(S) = \frac{0.66675}{s} + \frac{0.2165}{s^2} \quad (20)$$

The MSA for the given NTF is,

$$MSA = 0.9048V \quad (21)$$

Figure 7 below shows that the quantizer overloads when the input range exceeds a specific amplitude. The certain amplitude below which the quantizer will not saturate is the maximum stable amplitude (MSA).

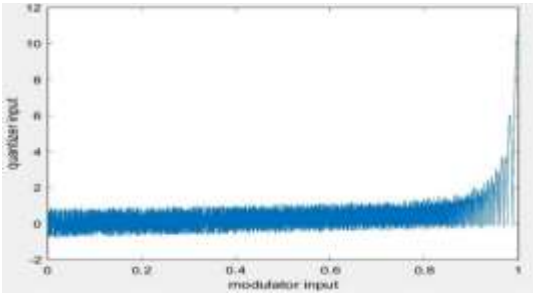

Fig. 7. Maximum Stable Amplitude (MSA) Estimation

C. Non-idealities of CT -SDM:

Practical continuous-time implementations suffer from the limitations of finite op-amps [9]: DC gain, limited gain-bandwidth product(GBW), and excess loop delay. Finite DC gain reduces NTF attenuation, degrading SNR. Limited GBW causes incomplete settling and distortion. Excess loop delay shifts poles toward the unit circle and may lead to instability. Therefore, minimum gain and bandwidth constraints are imposed to preserve stability and target resolution.

VI. Implementation of SDM

The Sigma-delta modulator is constructed using the Delta Sigma toolkit in MATLAB, with parameters such as resolution, bandwidth, quantizer bits, and oversampling ratio (OSR). The NTF, loop filter, filter coefficients, and loop topology are generated in MATLAB using the toolbox, with the above-mentioned parameters taken into account.

The sigma-delta modulator's analog blocks were implemented in Verilog A, and the Cadence Virtuoso tool was used for simulation to analyze the ADC's performance & determine the analog block specifications. These Verilog-A-programmed blocks were modelled to exhibit the same behaviour as a real analog circuit block.

The simulation results for the sigma-delta modulator are discussed, including its transient performance.

A. Second-order Sigma Delta ADC

The Error block, two Integrators, a Clocked Comparator, and a 1-bit DAC block in the feedback path make up the components of the 2nd-order SDM. All these blocks are programmed using Verilog-A and implemented in Cadence Virtuoso.

i. CT Integrator Modelling

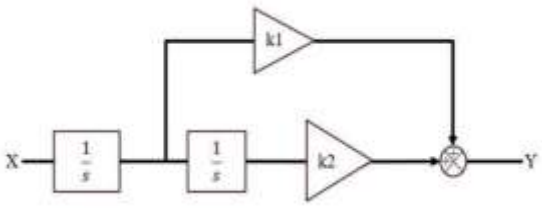

Fig. 8. CT Integrator modelling using CIFF architecture

The figure above shows the CIFF architecture implemented in 2nd-order SDM. The Discrete-Time NTF with OSR=128 and OBG=1.5 for a 2nd-order modulator is obtained using the CT Integrator model with the CIFF architecture. From DT NTF, the loop filter in discrete-time is estimated as $LZ = 1/(NTFZ - 1)$.

Using the DT loop filter, the continuous-time modulator's loop filter is estimated using the Impulse Invariant Transformation (IIT) technique, with an NRZ pulse applied to the DAC. The CT loop filter(L(s)) generated from the IIT technique is mentioned in equation (22),

$$L(S) = \frac{0.66675}{s} + \frac{0.2165}{s^2} \quad (22)$$

In equation (19) above, L(s) is the CT loop filter. Suitable values of K1 and K2 for the continuous time integrator in CIFF architecture, shown in Figure 8 from equation (22), are,

$$K1 = 0.6675 \quad (23)$$

$$K2 = 0.2165 \quad (24)$$

where, K1 and K2 are integrator gain coefficients

ii. Implementation of 2nd -order SDM in Cadence Virtuoso

Second-order SDM is simulated behaviorally using Verilog-A modules for the error block, integrator blocks, clocked comparator block, and 1-bit DAC block in Cadence Virtuoso. Integrators cascaded in a Feed-forward (CIFF) architecture are used for the given model. A sinusoidal signal of 900 mV amplitude and 1Hz frequency is taken as input to the 2nd-order SDM and sampled at a sampling frequency of 256Hz, giving an oversampling ratio (OSR) of 128. Suitable values of K1 and K2 are: K1 = 0.6675 and K2 = 0.2165 for the

Continuous-Time loop filter.

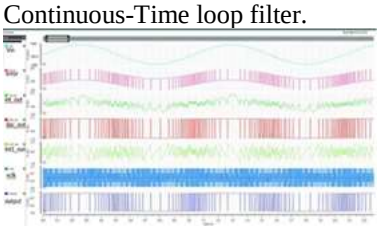

Fig. 9. Schematic of 2nd SDM with 900mVamplitude, 1Hz sinusoidal input signal in Cadence Virtuoso

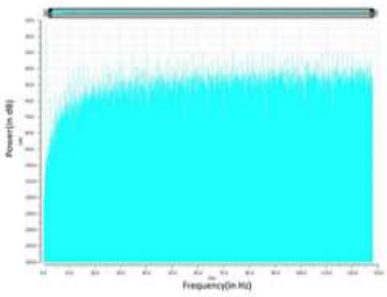

Fig. 10. Output Waveform of 2nd SDM with 1 Hz Sinusoidal, 900mV Amplitude input voltage for OSR=128 in Cadence Virtuoso

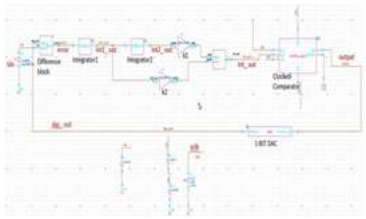

Fig. 11. FFT Spectrum of output of 2nd order SDM in Cadence

iii. Simulation Results of 2nd SDM with sinusoidal input in MATLAB

SNR was computed from FFT using 8192 samples using a Hanning window on the data received from Cadence, and signal power is extracted from the data, which is used to calculate the modulator's SNR and ENOB, and to find the FFT spectrum of 2nd-order SDM. SNR and ENOB obtained in Cadence using the Spectrum function, and MATLAB are tabulated below.

TABLE II. CALCULATED AND MEASURED VALUES OF PARAMETERS OF THE 2ND ORDER IN CADENCE VIRTUOSO AND MATLAB

Parameters	*Calculated*	*Measured (in cadence)*	*Measured (in MATLAB)*
Effective Number of Bits (**ENOB**)	15	14	14.0589
Signal-to-Noise Ratio (**SNR**) (in dB)	92.06	86.054	86.3944

B. Non-Linearities' Impact On Ctsdm's Performance

The effects of non-idealities, such as the Continuous-Time integrator's limited gain and gain bandwidth (GBW), on SDM performance will be covered here.

i. Impact of Integrator's Finite Gain on SDM Performance

The SNR is measured and tabulated for various integrator finite DC-gain values to describe the integrator's finite-gain impact on SDM performance.

TABLE III. EFFECT OF INTEGRATOR'S FINITE GAIN ON PERFORMANCE OF SDM

Finite DC Gain (A) (in dB)		*SNR (in dB)*
1st Integrator	*2nd Integrator*	
20	20	60.09
30	30	74.695
40	30	82.240
40	40	84.647

From the table, we observe that the SNR drops with the integrator's gain. To keep the SNR loss within 3dB, integrators must meet minimum gain criteria. Any nonidealities in the first integrator stage will immediately affect the modulator's SNR, so the first integrator has the highest gain requirement. The restrictions are progressively relaxed for the successive integrator stages.

ii. Impact of Integrator's Finite Gain Bandwidth (GBW) on SDM performance

The SNR is measured for different integrator GBW values and tabulated to assess the effect of integrator finite gain bandwidth (GBW) on modulator performance.

TABLE IV. IMPACT OF INTEGRATOR'S FINITE GAIN BANDWIDTH (GBW) ON SDM PERFORMANCE

Finite GDW	*SNR (in dB)*
f_s	82.31
$2f_s$	84.934
$3f_s$	85.01

From the table, we observe that the SNR drops with the integrator's GBW. To keep the SNR loss

within 3dB, the integrator's GBW product must be determined.

VII. Conclusion and Future Scope

A second-order continuous-time sigma-delta modulator based on the CIFF architecture was designed and validated at the system level. The architecture was synthesized using the MATLAB Delta-Sigma Toolbox and implemented behaviorally in Cadence Virtuoso using Verilog-A models. With an oversampling ratio and a 1-bit quantizer, the proposed modulator achieves an SNR above 86 dB and an ENOB of 14 bits. The impact of integrator finite DC gain and limited GBW on modulator performance was analyzed, and minimum design requirements were identified to maintain performance degradation within 3dB. The obtained results demonstrate that the proposed architecture is suitable for low-frequency, high-resolution sensing applications such as temperature measurement.

Future improvements include integrating an optimized digital decimation filter to create an ADC system. At the same time, the decimation filter removes high-frequency components above the signal band. Higher-order filters will improve SDM performance. This enables improving the output's SNR. Also, implementing low-power strategies during Sigma-Delta ADC design can help reduce power dissipation throughout the circuit. Additionally, SDM with a higher-order loop filter of greater than 2nd order and a multibit quantizer can be modelled to achieve very high resolution in the order of 18-20 bits with considerable power consumption using low-power strategies.

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