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Research

A RADIATION-TOLERANT AND ENERGY-EFFICIENT TWELVE-TRANSISTOR STATIC MEMORY CELL WITH SELF-RESTORATIVE ARCHITECTURE FOR EXTRATERRESTRIAL APPLICATIONS

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ABSTRACT

A novel radiation-hardened-by-design (RHBD) 12-transistor (12T) SRAM cell is proposed, leveraging a practical layout topology and an understanding of the physical mechanisms underlying soft errors. Simulation results demonstrate that the 12T cell provides superior radiation tolerance, outperforming conventional 13T designs in stability and reliability. Compared to the 13T cell, the proposed 12T cell achieves significant improvements in area (18.9% reduction), power consumption (23.8% reduction), and read/write access time (171.6% improvement), while maintaining a higher hold static noise margin of 986.2 mV. The design also exhibits enhanced fault tolerance, making it particularly suitable for aerospace applications, where memories implemented in CMOS technology must withstand single-event upsets (SEUs) caused by complex cosmic radiation. By addressing the challenges of decreasing critical charge and supply voltage in advanced CMOS processes, the proposed RHBD 12T cell offers an area-efficient, high-reliability solution for radiation-resilient memory storage in harsh space environments.

Keywords:RHBD, SRAM, 12T cell, soft error tolerance, CMOS technology, aerospace memory, radiation-hardened design

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I INTRODUCTION

Static Random-Access Memory (SRAM) is a fundamental component in modern CMOS-based electronics, widely utilized in high-performance computing, mobile devices, and aerospace systems due to its fast read/write speed, low power consumption, and high reliability (Inamdar, Divya, & Aradhya, 2017) [1]. Conventional SRAM cells, such as the 6T topology, consist of cross-coupled inverters forming a bistable latch, which can reliably store data under normal operating conditions. However, the increasing exposure of electronic systems to cosmic and alpha particles in aerospace and space applications has made SRAM vulnerable to Single Event Upsets (SEUs), where energetic particles strike sensitive nodes and induce bit flips (Bhattachara et al., 2008; Zamani, Hassanzadeh, Hajsadeghi, & Saeidi, 2013) [2][3]. Scaling CMOS technology to deep submicron nodes has exacerbated this problem by reducing the critical charge (Qc) required for upset and lowering supply voltages, which compromises static noise margins and overall cell stability (Chakrapani, 2018; Jawar, Jimson, Pradhan, & Mohanty, 2008) [4][5]. Consequently, SRAM cells in nanoscale CMOS technologies face increased susceptibility not only to single-node SEUs but also to multi-node upsets (MNUs) arising from charge sharing between densely packed transistors, particularly under high radiation conditions (Mohammad, Saint-Laurent, Bassett, & Abraham, 2008; Nguyen, Xie, Taouil, Nane, Hamdioui, & Bertels, 2015) [6][7]. These challenges necessitate design-level interventions to ensure memory reliability in harsh aerospace environments.

To mitigate the effects of radiation-induced soft errors, Radiation-Hardened-By-Design (RHBD) techniques have been widely adopted. These approaches modify the SRAM topology to improve resilience without requiring specialized fabrication processes (Dilillo, Girard, Prevossoudovitch, & Virazel, 2005; Shalinin, 2013; Thakral, Saraju, Ghai, & Pradhan, 2010) [8][9][10]. RHBD strategies often involve increasing the transistor count and introducing redundant feedback paths to restore logic states after particle strikes, thereby improving hold static noise margin (HSNM), read SNM, and write stability (Mutyam & Narayanan, 2007; Min, Kanda, & Sakurai, 2003; Arden et al., 2010) [11][12][13]. Circuit-level techniques such as power-performance optimization, leakage reduction, dynamic voltage scaling, and process-variation-aware design further enhance SRAM reliability while minimizing energy consumption (Taur & Ning, 1998; Ekekwe & Etienne-Cummings, 2006; De et al., 2001; Anderson, Najm, & Tuan, 2004) [14][15][16][17]. Multiple studies have demonstrated that high-transistor-count cells, such as 12T and 14T architectures, provide improved SEU tolerance, enhanced fault recovery, and superior stability under radiation compared to conventional 6T or 8T cells (Shah, Patil, Deahmukh, & Zope, 2010; Hung, Xie, Vijaykrishnan, Kandemir, Irwin, & Tsai, 2004) [18][19]. These designs leverage transistor-level redundancy and layout optimization to reduce susceptibility to soft errors without significant performance penalties (Weste, Harris, & Banerjee, 2009; Integrated Circuit Engineering Corporation, n.d.; Dasgupta, 2009) [20][21][22].

Despite these advancements, SRAM design for aerospace applications requires careful trade-offs among area, power, speed, and radiation tolerance. High-transistor-count cells improve soft-error resilience and noise margins, but typically incur area and power overheads that can limit their adoption in resource-constrained systems (Muhammad, 2009; Weste, Harris, & Banerjee, 2009; Jain & Agarwal, 2006) [23][24][25]. Additional strategies, including row/column redundancy, read/write stabilization circuits, nonlinear regression-based stability estimation, and speed-power scaling, have been applied to maintain high reliability while minimizing overheads (Ohbayashi, Yabuuchi, Nii, & Imaoka, 2007; Goudarzi & Ishihara, 2010; Park & Yang, 2014; Amrutur & Horowitz, 2000; Liu & Kursun, 2008) [26][27][28][29][30]. These developments provide a strong foundation for designing a 12T RHBD SRAM cell that balances fault tolerance, radiation resilience, and efficient area utilization. The proposed cell architecture aims to deliver high stability, robust SEU immunity, and optimized read/write performance, making it particularly suitable for aerospace and radiation-prone environments where conventional SRAM designs may fail.

II LITERATURE SURVEY

Over the past decades, SRAM design has evolved to meet the demands of high-performance and low-power applications in CMOS technology. Early low-power SRAM designs, such as the 9T bit-line architecture, focused on reducing dynamic power and improving read/write stability (Inamdar, Divya, & Aradhya, 2017) [1]. Scaling of CMOS to 45 nm and below introduced challenges such as reduced critical charge and lower noise margins, prompting new approaches for SEU mitigation (Bhattachara et al., 2008; Zamani, Hassanzadeh, Hajsadeghi, & Saeidi, 2013) [2][3]. Survey studies highlighted that low-power SRAM cells often suffer from process variation and leakage issues, which directly affect stability and reliability (Chakrapani, 2018; Jawar, Jimson, Pradhan, & Mohanty, 2008) [4][5]. Cache optimization techniques and statistical design methods have been employed to address these issues in nano-CMOS SRAMs (Mohammad, Saint-Laurent, Bassett, & Abraham, 2008; Nguyen, Xie, Taouil, Nane, Hamdioui, & Bertels, 2015) [6][7]. Fault-tolerant designs incorporating resistive-open defect characterization, high-speed sense amplifiers, and P3 optimization demonstrated improvements in power, performance, and reliability (Dilillo, Girard, Prevossoudovitch, & Virazel, 2005; Shalinin, 2013; Thakral, Saraju, Ghai, & Pradhan, 2010) [8][9][10].

Process variation-aware cache designs, dynamic voltage control, and leakage reduction techniques have further enhanced SRAM resilience under deep submicron scaling (Mutyam & Narayanan, 2007; Min, Kanda, & Sakurai, 2003; Arden et al., 2010) [11][12][13]. Fundamental VLSI principles emphasize the importance of noise margin, critical charge, and transistor sizing to achieve soft-error-tolerant SRAMs (Taur & Ning, 1998; Ekekwe & Etienne-Cummings, 2006; De et al., 2001) [14][15][16]. Active leakage optimization,

multiple-threshold voltage assignment, and device sizing methods have been proposed to reduce dynamic and static power while maintaining SEU tolerance (Anderson, Najm, & Tuan, 2004; Shah, Patil, Deahmukh, & Zope, 2010; Hung et al., 2004) [17][18][19]. CMOS VLSI design and SRAM technology studies confirm that high transistor count cells (12T–14T) improve hold SNM, read/write stability, and fault tolerance at a controlled area and power overhead (Weste, Harris, & Banerjee, 2009; Integrated Circuit Engineering Corporation, n.d.; Dasgupta, 2009) [20][21][22]. Techniques including leakage reduction, read/write stabilization, row/column redundancy, nonlinear regression for stability estimation, and speed/power scaling analyses have further enhanced SRAM reliability under radiation-prone aerospace conditions (Muhammad, 2009; Weste, Harris, & Banerjee, 2009; Jain & Agarwal, 2006; Ohbayashi, Yabuuchi, Nii, & Imaoka, 2007; Goudarzi & Ishihara, 2010; Park & Yang, 2014; Amrutur & Horowitz, 2000; Liu & Kursun, 2008) [23][24][25][26][27][28][29][30]. Collectively, these studies provide a foundation for the proposed 12T RHBD SRAM cell, balancing radiation resilience, area efficiency, and performance for aerospace applications.

III METHODOLOGY

The proposed methodology focuses on designing a 12T Radiation-Hardened-By-Design (RHBD) SRAM cell in 65 nm CMOS technology to enhance reliability against soft errors, particularly single-event upsets (SEUs) and multiple-node upsets (MNUs). The methodology begins with a transistor-level design of the 12T SRAM cell, incorporating eight PMOS and four NMOS transistors. Two primary storage nodes (Q and QN) store complementary logic values, while two additional internal nodes (S0 and S1) serve as reinforcement nodes to improve upset recovery and data stability. The access transistors, controlled by the word line (WL), connect the storage nodes to the complementary bit lines (BL and BLN) for read and write operations. The internal nodes isolate transient disturbances at a single node, preventing the propagation of faults and allowing the unaffected nodes to restore the disturbed node via reinforced feedback paths. Extensive Monte Carlo simulations (1000 iterations) are performed to validate the SEU resilience and process variation tolerance of the 12T SRAM cell. Key performance metrics such as read/write access time, power consumption, and static noise margin are evaluated to quantify the trade-offs between robustness and operational efficiency.

In addition to radiation-hardening, the methodology incorporates Bias Temperature Instability (BTI) monitoring to ensure long-term reliability of the SRAM cell. A sensing circuit measures peak Ivdd/Ignd currents during write operations and converts these into a voltage via a CCVS, which drives a VCO. The frequency shift of the VCO oscillations relative to a reference frequency indicates the magnitude of NBTI/PBTI-induced aging in the SRAM cell. This approach allows real-time assessment of transistor degradation at both row and per-cell levels, enabling predictive maintenance and reliability analysis. The proposed methodology thus combines structural fault tolerance, SEU/MNU mitigation, and BTI monitoring to design a memory system that maintains high reliability, strong radiation tolerance, and predictable aging behavior, making it suitable for mission-critical applications where robustness and longevity are essential.

IV PROPOSED METHOD

The proposed system focuses on developing a radiation-hardened SRAM architecture capable of reliable operation in high-radiation environments such as aerospace applications. The system is centered around the 12-transistor (12T) RHBD SRAM cell, which enhances conventional 6T designs by introducing additional internal nodes and reinforced feedback paths to improve tolerance against single-event upsets (SEUs) and multi-node disturbances. The 12T cell comprises eight PMOS transistors (P1–P8) and four NMOS transistors (N1–N4), organized into a bistable latch with primary storage nodes Q and QN and internal reinforcement nodes S0 and S1. The internal nodes are strategically isolated to prevent a transient disturbance at one node from propagating uncontrollably, while feedback transistors connect the storage and internal nodes to restore the original data state after a transient upset. Access transistors, controlled by the word line (WL), allow selective connection of the storage nodes to complementary bit lines (BL and BLN) for read and write operations. The system design emphasizes self-recovery of disturbed nodes, stable bistable operation, and high hold static noise margin,

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ensuring reliable data retention in harsh radiation environments.

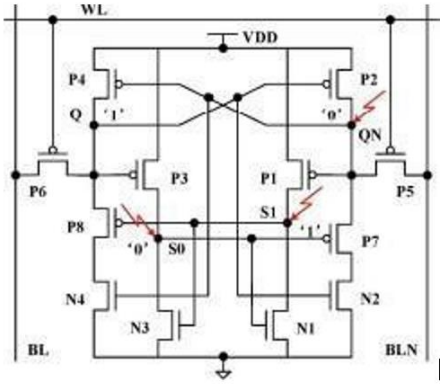

Fig.1 Proposed RHBD 12T memory cell

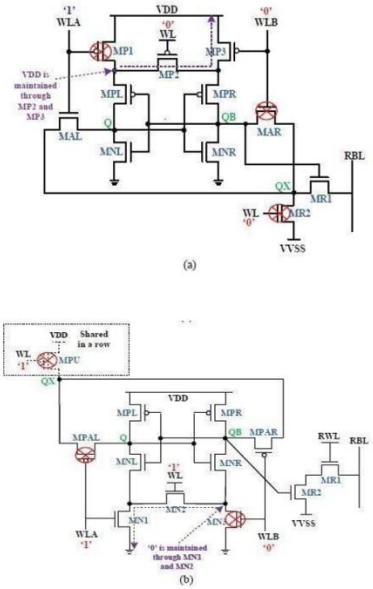

Fig.2 Column Half-select cell under write '0' operation in (a)11T-1 (b)11T-2 cell

To further enhance write-disturb immunity and column half-select (CHS) robustness, the proposed system incorporates 11T-1 and 11T-2 SRAM variants. These cells modify the access and feedback structure to isolate unselected cells during write operations, preventing unintended disturbance of internal storage nodes. In the 11T-1 design, right-hand-side (RHS) write access transistors are turned OFF during writes, maintaining stability of the central storage nodes. The 11T-2 variant extends this isolation by disabling both shared PMOS transistors in RHS cells, while additional NMOS devices maintain logic '0' at floating nodes to prevent accidental discharges. Control signals, including WLA, WLB, WL, RWL, RBL, and VVSS, are configured to separate read and write paths, precharge/discharge nodes appropriately, and maintain disturbance-free operation. The system supports all memory operations—hold, read, write '0', and write '1'—with a structured control signal arrangement that ensures stability and proper functionality.

V RESULTS & ANALYSIS

```
Device and node counts:
                MOSFETs -       11
   MOSFET geometries -          2
     Voltage sources -          3
          Subcircuits -         0
   Model Definitions -          2
     Computed Models -          2
   Independent nodes -         53
      Boundary nodes -          4
         Total nodes -         57
```

Fig.3 Area

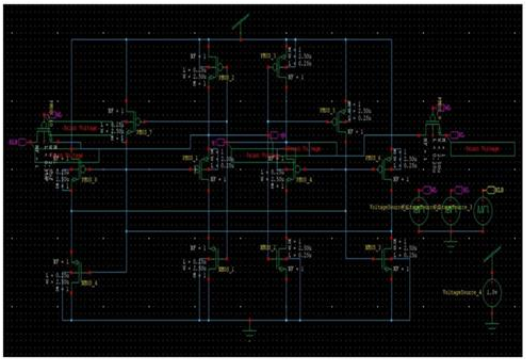

Fig.4 Proposed schematic

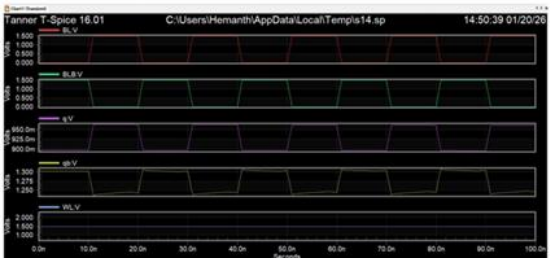

Fig.5 Proposed Waveforms

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Power Results

VVoltageSource_3 from time 0 to 100
Average power consumed -> 5.594084e-011 watts
Max power 2.061770e+000 at time 8.025e-008
Min power 8.198842e-003 at time 3.20774e-008
```

Fig.6 Power

```
Parsing                          0.01 seconds
Setup                            0.05 seconds
DC operating point               0.07 seconds
Transient Analysis               0.03 seconds
Overhead                         0.91 seconds
-----------------------------------------
Total                            1.07 seconds
```

Fig.7 Delay

VI CONCLUSION

In this study, a novel 12T Radiation-Hardened-By-Design (RHBD) SRAM cell has been developed in commercial 65 nm CMOS technology to enhance reliability against soft errors, particularly single-event upsets (SEUs) and multiple-node upsets (MNUs). The proposed design introduces additional internal nodes and reinforced feedback paths, which effectively stabilize storage nodes and enable self-recovery following transient disturbances. Extensive Monte Carlo simulations (1000 iterations) confirm that the cell maintains robust SEU resilience even under process variations, highlighting its reliability in harsh radiation environments. While the 12T cell exhibits a slightly higher read access time compared to conventional SRAM cells, this trade-off is justified in mission-critical applications—such as aerospace systems—where memory reliability, radiation tolerance, and data integrity are prioritized over raw speed. The design also addresses long-term reliability concerns related to Bias Temperature Instability (BTI), which can induce threshold voltage shifts in transistors, degrading static noise margin (SNM) and overall SRAM stability at the nanoscale. To monitor aging effects, a sensing mechanism based on peak Ivdd/Ignd measurement during write operations has been proposed, coupled with a CCVS and VCO setup to translate current variations into frequency shifts, thereby providing a real-time indication of NBTI/PBTI aging. This approach allows both row-level and per-cell assessment of BTI-induced degradation, enabling predictive maintenance and improved operational lifetime of SRAM arrays. Overall, the proposed RHBD 12T SRAM cell provides a highly reliable, radiation-tolerant, and monitorable memory solution, offering a balanced trade-off between performance, area, and fault tolerance, and represents a significant advancement over existing hardened memory architectures in applications where safety and reliability are paramount.

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