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Research Paper

DESIGN AND ANALYSIS OF A 4-BIT ASYNCHRONOUS COUNTER USING SENSE-AMPLIFIER BASED FLIP-FLOPS

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ABSTRACT

The Cadence EDA tool was used for all design and simulation work on the Sense-Amplifier- Based Flip-Flop (SAFF) for low-voltage operation. Traditional flip-flop designs frequently experience issues including poor noise margins, increased latency, and unreliable switching as contemporary VLSI systems continue to operate at lower supply volages to reduce power consumption. These problems are mitigated by sense-amplifier-based flip-flops, which are ideal for low-voltage applications because they can precisely detect minute voltage changes.The design and implementation of a 4-bit asynchronous counter employing an is the main goal of this project.

This project compares the performance of a transmission-gate flip-flops (TGFFs) with a 4-bit asynchronous counter developed using the suggested SAFF architecture. The synchronous counter's design guarantees simultaneous switching and prevents the ripple delay present in asynchronous counters because all of its flip-flops are powered by a single clock. The Cadence Virtuoso environment is used for the evaluation, which focuses on crucial factors including power consumption, propagation latency, and dependability at lower supply voltages.

According to simulation studies, the SAFF-based counter outperforms the TGFF-based design in terms of power consumption, speed, and dependability at low voltages. Overall, this effort shows that the suggested SAFF-based counter is an appropriate and economical choice for near- threshold and low-power VLSI applications.

Keywords: Sense Amplifier Based Flip-Flop (SAFF), 4-Bit Synchronous Counter, Low-Voltage Operation, Low-Power VLSI Design, TGFF, Cadence Virtuoso, CMOS Digital Circuit

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I INTRODUCTION

As the Internet of Things (IoT) continues to advance rapidly, there has been a substantial increase in demand for low-power and cost-effective system-on-chip (SoC) solutions. This shift has made power and area efficiency the main focus in design, overtaking speed as the key research priority. In scenarios where performance is not the critical factor, one of the most effective ways to reduce energy consumption is by lowering the supply voltage, even if it leads to a decrease in operating speed. As a result, there has been a growing interest in digital circuit design techniques that operate at subthreshold and near-threshold voltages [1, 2]. The sense- amplifier-based flip-flop (SAFF) consists of a differential sense-amplifier (SA) stage followed by an RS-latch [3–5]. However, at low supply voltages, the SA stage may latch incorrect data due to reduced voltage headroom and transistor mismatch. To address these challenges, a low-voltage SAFF with transition completion detection (TCD) was proposed in [5, 6]. This design utilizes a detection signal generated to indicate the completion of the SA transition, thereby mitigating yield degradation. While the negative setup time enables operation at lower voltages compared to conventional transmission-gate flip-flops (TGFFs), the additional circuitry increases both power consumption and area. In this paper, we propose a novel area- and energy-efficient SAFF with a TCD scheme to overcome these limitations at lower supply voltages.

II LITERATURE SURVEY

Author(s)	Year	Focus Area	Application	Limitations
David Chaum	2004	Cryptographic voting protocol	Secure electronic voting	High computational complexity and implementation difficulty
Ron Rivest	2006	Voter-verifiable audit trails	Transparent EVM systems	Increased cost and mechanical complexity
Ariel J. Feldman et al.	2007	EVM security analysis	Security evaluation of voting machines	Identified flaws without full mitigation solution
Aviel Rubin	2002	Software security in EVMs	Secure voting software	Mainly theoretical, limited practical validation
Neal McBurnett	2009	Open-source voting systems	Transparent electronic voting	Vulnerable to hardware-level attacks
Josh Benaloh	2005	Cryptographic vote verification	Voter-verifiable elections	Requires advanced cryptographic knowledge

III EXISTING SYSTEM

The Transmission-Gate flip-flops (TGFF) design is shown in Figure 1. To achieve high-speed operation and lower clock power consumption, the suggested flip-flop combines a sense-amplifier based latch with a clocked input buffering step.

Three primary functional blocks make up the TGFF architecture: an output storage stage,a sense-amplifier latch, and a timed input buffer. By separating the data input from the internal nodes while the clock is not in use, the timed input buffer minimizes needless switching and lowers dynamic power dissipation. Complementary clock signals (CLK and $C\bar{L}K$) are applied to ensure correct data sampling and regulated signal propagation.

The primary component of the TGFF is the sense-amplifier latch. By using differential input signals (D and DB), it enhances noise immunity and facilitates quick evaluation. The sense amplifier detects and amplifies the tiny voltage difference between the differential inputs during the active clock phase. Set-bar (SB) and reset-bar (RB) are examples of control signals that help speed up the evaluation process and guarantee proper logic resolution.

Cross-coupled inverters are used to implement the output latch, which stores the evaluated data. When the clock is turned off, this step maintains the logic state and produces steady complementary outputs (Q and QB). The output buffering ensures sufficient drive intensity for following logic stages without imposing additional strain on the sense-amplifier stage.

Block Diagram

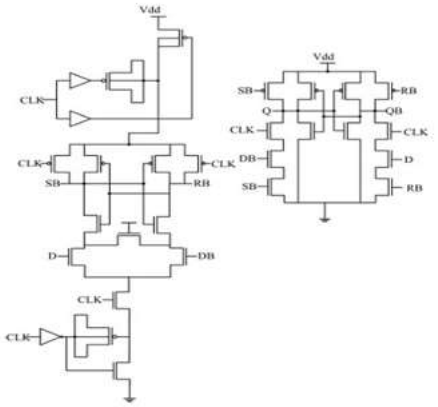

Fig 1: EXISTING TGFF SENSING STAGE AND LATCHING STAGE (TGFF)

IV PROPOSED SYSTEM

Figure 1a illustrates the circuit structure of the SAFF-TCD design [5, 6]. The transition completion (TC) signal is generated using a 2-input NAND gate, which takes the SA stage outputs (RB and SB) as inputs. During the SA stage operation, both RB and SB are pre charged to high when the clock signal (CK) is low, ensuring that TC remains at low. When CK transitions to high, the completion of the SA stage transition causes one of RB or SB to switch to low, there by setting TC to high, Consequently, transistor Mn X remains off during the SA stage transition and turns on only after the transition is complete. A similar detection mechanism was previously proposed in [7], utilizing an XOR gate instead of a NAND gate, as shown in Figure 1b. In this design, the TC signal distance travelled, and passengers would enter and depart stations using RFID-enabled smart cards or tags. This technology seeks to improve productivity, decrease human error, and streamline the metro experience.

(CBG) is generated only when the input data changes after the CK trigger, leading to lower power consumption. However, despite using transistor merging techniques, the advantage of low power is diminished due to the excessive number of transistors. Figure 2a shows the concept of the proposed design. In our design, we use De Morgan's law to replace the original NAND gate with an OR gate and two inverters. This technique enables the successful integration of the OR gate and inverters into the SA and latch, respectively, using only two nMOS transistors (MnR and MnS) to implement the OR

gate and two pMOS transistors (Mp1 and Mp2) to implement the inverters, as shown in Figure 2b. Therefore, our design requires only 23transistor, providing superior performance and a better layout area. The operating principles of the proposed design are as follows: when CK is low, both RB and SB are pre charged to logic high, turning off transistors MnR and MnS. When CK transitions to high, one of RB or SB switches to logic low, turning on either MnR or MnS during the rising edge of CK. These transistors remain active only after the SA stage transition is complete. Figure 2c provides a detailed record of the corresponding actions of the proposed detection circuit when the input signal Din changes after the CK trigger.

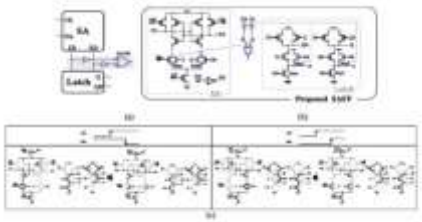

FIGURE 2 | Proposed SAFF design.

V SIMULATION DIAGRAMS

A master–slave test system was employed to evaluate the performance differences between the proposed design and existing flip-flop (FF) architectures. The TGFF design was implemented using the TSMC 16 nm CMOS process technology. To ensure a fair comparison, all transistors were configured with a 4-fin structure and identical layout height. Designs [4] and [5] were excluded from the comparison because they are unable to operate reliably at low supply voltages. To specifically investigate low-voltage performance, simulations were conducted at 10 MHz with a supply voltage of 0.4 V. Additionally, each FF was configured to drive identical FO4 loads to maintain consistency in performance evaluation.

The key parameters of all FF designs are summarized in Table 1. By incorporating the TCD circuit scheme, the proposed design achieves superior power efficiency in terms of average power consumption compared to designs [6] and [7]. At a switching activity of 25%, the proposed design reduces average power consumption by 16.6%, 25.8%, and 16.2% compared to TGFF, design [6], and design [7], respectively. Leakage power results, also listed in Table 1, indicate that the proposed design achieves the lowest leakage power, whereas design [7] exhibits the highest leakage due to its complex circuit structure. Although the TCD technique increases circuit complexity—resulting in the longest hold time in design [7]—both the proposed design and design [6] demonstrate nearly zero setup time. In contrast, design [7] exhibits a positive setup time due to the delay introduced by its TCD circuitry waiting for the input signal (Din). TGFF shows a longer DQ delay compared to SAFF design [8] because of its relatively larger positive setup time. Furthermore, the proposed design achieves the best power–delay product (PDP), showing a 47.5% reduction compared to design [6] at 25% switching activity.

Figure 3 presents the SA output waveforms of designs [6], [7], and the proposed design at VDD = 0.35 V. The results demonstrate correct output generation for the proposed design and design [6], whereas design [7] exhibits inaccuracies. Figure 4 illustrates the average power consumption under varying input data switching activities. The proposed design consistently outperforms the others across all switching probabilities, except when the switching probability is zero. Finally, Figure 5 shows the layout schematics of the SAFF designs. Owing to reduced transistor count and optimized layout structure, the proposed design achieves the most compact area. Compared to design [7], the proposed layout achieves up to 38.7% area savings.

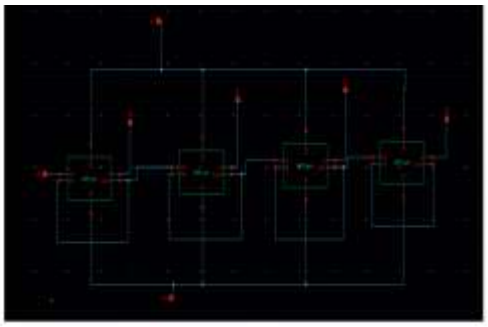

Fig 3. SAFF

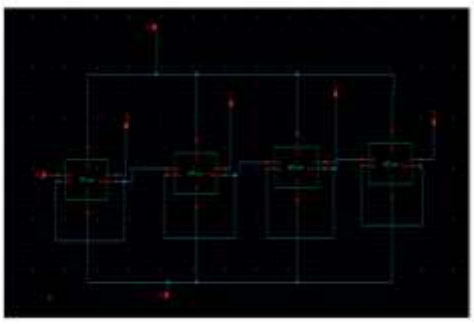

Fig 4. 4-Bit Asynchronous Counter

VI RESULTS

The power consumption of the proposed SAFF-

based counter is drastically reduced compared to the existing TGFF-based design.

The silicon area required for the proposed counter is lower, contributing to better area efficiency.

The combined reduction in power and area makes the proposed design more suitable for low-power and high-performance applications.

The results confirm that replacing conventional flip-flops with sense- amplifier based flip-flops leads to significant energy savings in asynchronous counter implementations.

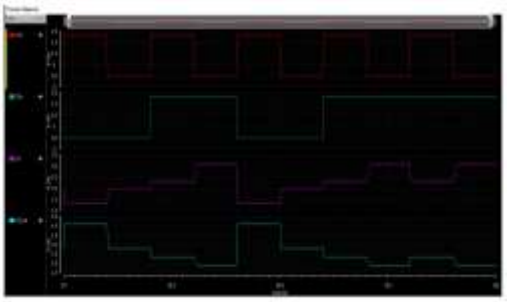

Fig 5. SAFF SIMULATION RESULTS

Fig 6. 4-Bit Asynchronous Counter

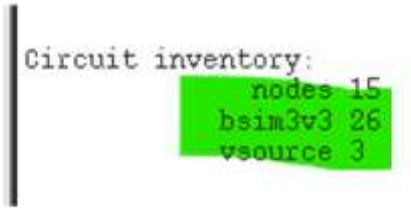

Fig 7. Area

Fig 8. Power

Fig 9. COMPARISSION OF TGFF & SAFF

VII CONCLUSION

A novel sense-amplifier-based FF with a TCD scheme that is both area- and power-efficient is suggested. By employing0020a logic- and circuit-level integration approach, our design reduces the excessive area of prior designs while significantly decreasing power consumption. The suggested FF achieves the maximum energy efficiency among the compared designs, according to evaluation data. Owing to its greater area and power efficiency, the proposed FF is perfect for low-area, low-power IoT applications.

REFERENCES:

[1].H. Kaul, M. Anders, S.Hsu , A. Agarwal, R. Krishnamurthy, and S. Borkar, “Near- Threshold Voltage (NTV)Design Opportunities and Challenges,” in Proceedings of the IEEE Design Automation Conference, (IEEE,2012),1149–1154.

[2] D.Jeon ,M.Seok, C.Chakrabarti D.Blaauw, and D.Sylvester ,“A Super Pipelined Energy Efficient Subthreshold 240 MS/s FFT Core in 65 Nm CMOS,” IEEE J Solid State Circuits 47, no. 1 (January 2012): 23–34.

[3] J. Montanaro, R. T. Witek, K. Anne, et al., “A 160-MHz, 32-b, 0.5-W CMOSRISC Microprocessor,” IEEE Journal of Solid-State Circuits 31, no.11 (November 1996): 1703–1714.

[4] B. Nikolic, V. G. Oklobdzija, V. Stojanovic, W. Jia, J. K.-S. Chiu, and M.Ming-Tak Leung, “Improved Sense-Amplifier-Based Flip-Flop: Design and Measurements,” IEEE Journal of Solid-State Circuits 35, no. 6 (June 2000): 876–884.

[5] A. G. M. Strollo, D. De Caro, E. Napoli, and N. Petra, “A Novel High-speed Sense-Amplifier-Based Flip-Flop,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems 13, no. 11 (November 2005): 1266–1274.

[6] S. Kim, et al., “Ferroelectric FET Nonvolatile Sense-Amplifier Based Flip- Flops for Low Voltage Operation, IEEE Transaction Circuits and Systems I: Regular Papers 71 (November 2023): 274–286.