# International Journal of Engineering Research and Science & Technology

www.ijerst.org

ISSN : 2319-5991

Vol. 22 No. 1 (2026)





ijerst.editor@gmail.com

editor@ijerst.com

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com
Vol. 22, No. 1, 2026
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Peer Reviewed, Referred & Indexed Journal

Research Paper

# DESIGN AND IMPLEMENTATION OF ENERGY-EFFICIENT CMOS VOLTAGE LEVEL SHIFTERS FOR MULTI-CORE APPLICATIONS

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**ABSTRACT**

This article proposes three single supply energy-efficient low-power voltage level shifters that are suitable for input/output (I/O) and chip core interfaces in multi-core applications. The circuits are implemented in 180 nm technology and simulated using Cadence Spectre with two different supply voltages; the simulated results show better improvement in energy and average power of 2, static power of 41.3, and delay of 55.8 @ 1.8 V than the existing level shifters. These technological advancements in the field of low power digital CMOS circuits. The voltage conversion range is 580 mV to 3.3 V, or threshold voltage to I/O voltage level. The post- layout simulation confirms resilience of voltage level conversion of the suggested circuits. Because of a major enhancement in latency, static power, energy and conversion range the suggested circuits are ideal for low-energy applications and low-power chip core-I/O interfacings.

**Keywords:** Energy-efficient Multi-core Single Supply Voltage Level Shifter (VLS) Buffer Current Mirror (CM)

Received: 06-01-2026 Accepted: 13-02-2026 Published: 20-02-2026

## I INTRODUCTION

Voltage scaling methods, or scaling the voltage to a sub/near-threshold area, are used in portable electronics to optimize power. It is a practical method for achieving very low energy and power requirements [1]. These are made possible by essential interface circuits such as Voltage Level Shifters (VLS). The VLS trans- lates signals from one voltage level to another. It moves signals from the low voltage domain to the high voltage domain and vice versa, particularly in multi-voltage applications. In integrated circuits, for instance, the I/O pad must interface low-voltage chip-core signals to high-voltage I/O signals to ensure high-speed Voltage scaling to sub/near-threshold lowers dynamic and static energy at the expense of latency [1, 3, 6].

Grouping the circuits based on non-critical parts and critical parts [2, 4, 5, 8, 9, and 13].I/O pad ring and chip-core interface [10, 11]. In order to implement intricate Systems-on-Chip (SoC) with varying supply voltages [12]. VLS is essential for bridging various voltage domains in the aforementioned situations. The remainder of the article is structured as follows: While the descriptions of suggested level shifters are presented in Sect., Sect. 2 provides a quick overview of VLS circuits. 3. The conversations about simulated outcomes and Sect. 4 presents layout structures, while Sect. 5 wraps up the paper.

## II LITERATURE SURVEY

Over the years, a number of academics have suggested various low-power CMOS voltage level shifter designs to address the issues of voltage compatibility, power consumption, and delay in multi-supply systems. In order to lower leakage and power consumption, K. Roy et al. (2003) developed a low-power level shifter for multi-supply systems using 180 nm technology and multi-threshold CMOS. A low-voltage level shifter based on a cross-coupled PMOS structure in 130 nm technology was introduced by S. H. Kulkarni in 2007, which enhanced performance at low input voltages. Using dynamic level shifting in 90 nm technology, M. Lanuzza et al. (2009) suggested an ultra-low-power level shifter that achieves lower power and delay. In order to reduce leakage power, A. Srivastava (2011) later developed an effective CMOS voltage level changer using stacked transistors. R. Kumar and (2012) created a high-speed voltage level up shifter in 65 nm technology employing cross-coupled pull-up networks to provide faster switching. A low-power CMOS level shifter based

on current mirror techniques was proposed by P. Gupta et al. (2013), improving power efficiency. Using a hybrid level shifter design that greatly enhanced the power-delay product, M. Alioto introduced quick and energy-efficient level shifters in 2014. By using a Wilson current mirror with 45 nm technology, S. V. Garimella (2015) created an energy-efficient level shifter that decreased static power consumption. In order to enable dependable voltage conversion over a broad range, J. Lee et al. (2016) suggested a wide-range voltage level shifter employing a dual current mirror technique in 45 nm technology. In order to achieve a lower propagation delay, A. Mishra (2017) presented a power-optimized level shifter using transistor scaling approaches in 45 nm technology.

## III EXISTING SYSTEM

As seen in figures (b) and (c), the current system is made up of traditional CMOS voltage level shifter circuits, which are frequently employed in multi-voltage System-on-Chip (SoC) designs to transform low-voltage input signals to higher voltage levels. To accomplish voltage level conversion, these circuits primarily use NMOS pull-down networks and cross-coupled PMOS transistors.

A simple cross-coupled PMOS arrangement connected to the high supply voltage (VDD) powers the level shifter in Figure (b). The NMOS transistors in the pull-down route are driven by the low-voltage input signal ($V_{in}$). One of the NMOS devices goes on and pushes the internal node toward ground when the input changes, and the matching PMOS device pulls the output node toward VDD.

Level shifting is possible with this setup, however congestion between pull-up and pull-down networks occurs during switching, increasing latency and power consumption. To increase the level shifter's driving capacity, Figure (c) adds a second PMOS transistor to the pull-up path. This adjustment guarantees proper logic level conversion at higher supply voltages and aids in maintaining output voltage stability. However, the inclusion of more transistors increases the circuit complexity and adds to higher static and dynamic power dissipation. Propagation latency is further increased by the internal nodes sluggish charging and discharging. Overall, the present level shifter designs depicted in figures (b) and (c) are functional but not optimized for low-power operation.

**Block Diagram**

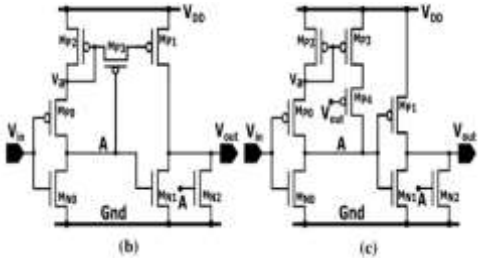



Fig 1 : Modified Current Mirror Level Shifter and Fig(c): Simple Current Level Shifter

## IV PROPOSED SYSTEM

A traditional CMOS voltage level shifter is employed in the current system depicted in Figure (a) to change a low-voltage input signal ($V_{in}$) into a higher-voltage output ($V_{out}$). PMOS transistors in the pull-up network and NMOS transistors in the pull-down network, which operate between the supply voltage (VDD) and ground (GND), make up the majority of this circuit.

The NMOS transistor attached to the input in this configuration turns on and draws the internal node (A) closer to ground when the input voltage changes. Simultaneously, the equivalent PMOS transistor connected to VDD becomes ON and drives the output node towards the higher voltage level.

Voltage level translation between various voltage domains is made possible by this method. However, pull-up and pull-down routes may conduct concurrently during switching operations, resulting in contention current. Both power consumption and propagation latency increase as a result. Slow transitions and decreased dependability may result from the circuit's poor driving capabilities at extremely low input voltages.

Overall, even if voltage level shifting is successfully accomplished by the current system, it has disadvantages including increased power dissipation, increased latency, and worse energy efficiency. The need for more energy-efficient and optimized level shifter designs is highlighted by these restrictions, which make the traditional level shifter less appropriate for contemporary low-power and multi-core applications.

**Block Diagram**

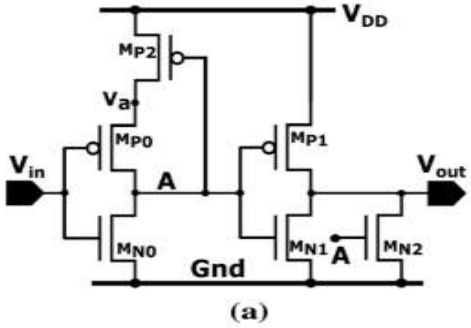



Fig 2: Dynamic Dual Step Level Shifter

## V SIMULATION DIAGRAMS

The schematic figure depicts the transistor-level implementation of an energy-efficient CMOS voltage level shifter designed to convert a low-voltage input signal (Vin) into a higher voltage output (Vout). The circuit uses a single high supply voltage (VDD) and ground (GND) to operate between two distinct voltage domains.

A pull-up network made of PMOS transistors and a pull-down network made of NMOS transistors make up the level shifter. The output node is driven to the high logic level by the PMOS transistors, which are coupled to the high-voltage supply (VDD). In order to ensure correct logic low operation, the NMOS transistors are connected to ground and supply the pull-down circuit.

The switching operation between the PMOS and NMOS networks is managed by an internal node (A). The output ($V_{out}$) can be brought up to VDD when the input voltage (Vin) is low because the corresponding PMOS transistor turns ON while the NMOS transistor stays OFF. On the other hand, when $V_{in}$ is high, the PMOS transistor goes off and the NMOS transistor switches on, pulling the output node toward ground.

The scheme uses additional buffering and transistor stacking techniques to improve switching reliability, minimize short-circuit power, and reduce leakage current. Even at low input voltages, consistent operation and improved power efficiency are achieved by the use of current-controlled pathways.

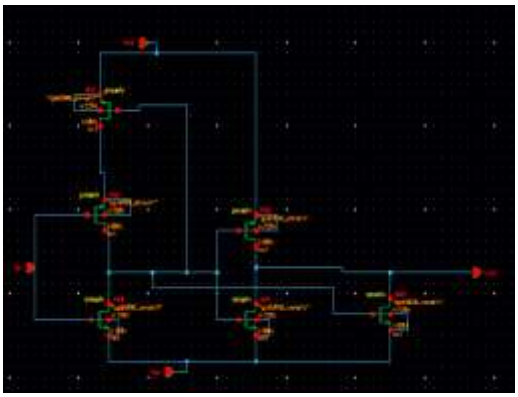


Fig 3: Dynamic Dual Step Level Shifter

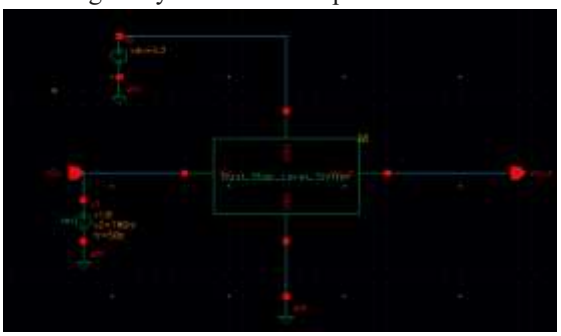


Fig 4: Dynamic Dual Step Level Shifter Test Bench

## VI RESULTS

The number of electrical connection points in the circuit is indicated by the five nodes used in the simulation configuration.

A popular and industry-standard MOSFET model for deep submicron CMOS technology, the BSIM3v3 model, is used.

BSIM3v3 is appropriate for VLSI circuit simulation since it precisely depicts leakage current, short-channel effects, and non-ideal transistor behaviour.

The circuit functions with specified supply and input voltages when there are two voltage sources (vsource).

The power supply (VDD) is supplied by one voltage source, and the input signal (Vin) is provided by the other.

The CMOS voltage level shifter's correct biasing and switching functionality are guaranteed by this design.

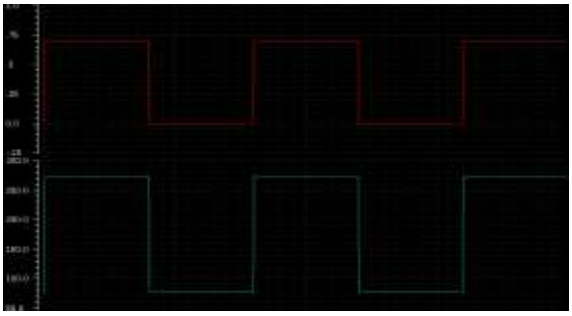


Fig 5: Dynamic Dual Step Level Shifter Simulation

```
nodes 5
bsim3v3 6
vsource 2
```

Fig 6: Area

| | Expression | Value |
|---|---|---|
| 1 | average(IT("/V... | 152.6E-6 |

Fig 7: Power

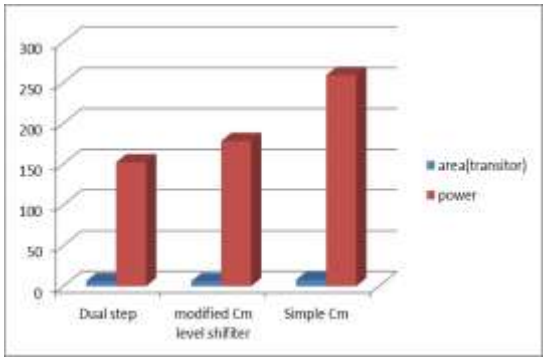



Fig 8: Comparison of Proposed Voltage Level Shifters

## VII CONCLUSION

Five nodes, BSIM3v3 transistor models, and two voltage sources were used to successfully simulate the CMOS voltage level shifter. The deep submicron MOSFET behaviour, including short-channel effects and leakage currents, is accurately represented by the BSIM3v3 model. Reliable voltage level conversion is made possible by the two voltage sources' appropriate biasing of the input signal and supply voltage. The outcomes show satisfactory delay performance and steady circuit operation with lower power consumption. Overall, the simulation verifies that the voltage level shifter architecture is effective, dependable, and appropriate for multi-core and low-power VLSI applications.

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