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Research Paper

DESIGN AND SIMULATION OF MOD-10 SYNCHRONOUS COUNTERS USING DUAL-LATCH FLIP-FLOPS

[1]B. RAJASEKHAR, [2]Dr.S.V.V.N. CHANUKYA PADIRA, [3]M. ANIL, [4]P. MURALI KRISHNA, [5]K. VEERANJANEYULU

[2]Associate Professor, ECE Dept, RISE Krishna Sai Prakasam Group of Institutions, Valluru, AP

[1,3,4,5]Students, ECE Dept, RISE Krishna Sai Prakasam Group Of Institutions, Valluru, AP

[1]boyar0158@gmail.com,[2]chanukya140@gmail.com,[3]anilmanjula7670@gmail.com,[4]muralikrishnapalakuri1@gmail.com,[5]veeranjaneyulurockey@gmail.com

ABSTRACT

In this project, a MOD-10 synchronous counter using twin latch flip-flops is designed and simulated. One common sequential circuit is the MOD-10 counter, which counts from 0 to 9 before resetting to zero. In contrast to traditional flip-flop-based counters, the suggested design uses dual latch flip-flops with sensing and latching stages to enhance timing performance. By ensuring that all state changes take place concurrently with the clock edge, synchronous operation minimises propagation time and prevents ripple effects. Dual latch flip-flops separate data capture from output transitions, resulting in glitch-free operation and improved synchronisation. After the count reaches decimal nine, reset logic is used to guarantee correct rollover. To ensure proper counting behaviour, digital design tools are used to construct and simulate the entire counter circuit.

Keywords: MOD-10 Synchronous Counter, Dual Latch Flip-Flop, Sequential Circuits, Synchronous Counting, GlitchFree Operation, Digital Logic Design, Reset Logic, Timing Performance.

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I INTRODUCTION

Digital systems represent the backbone of modern electronic technology, enabling computation, control, communication, and automation across a wide range of applications. Sequential circuits, which can store and analyse data across time, are the foundation of these systems. Sequential circuits rely on both current inputs and previous states, in contrast to combinational circuits that only generate outputs depending on present inputs. Counters are one of the most basic and popular sequential circuits. They are used in digital systems to divide frequencies, count occurrences, measure time, and produce control signals. Digital clocks, watches, timers, frequency synthesisers, data acquisition systems, microprocessor-based controllers, and communication devices all make considerable use of counters. The whole performance of the embedded system is directly impacted by the accuracy, speed, and dependability of these counters. In general, counters can be divided into two categories: synchronous counters and asynchronous (ripple) counters. Only the first flip-flop in an asynchronous counter receives the clock signal; each flip-flop's output serves as the clock input for the subsequent stage. Despite being straightforward and requiring minimal hardware, this method is not appropriate for high-speed applications due to cumulative propagation delay and timing uncertainty. Synchronous counters, on the other hand, guarantee that state transitions take place at the same moment by applying the clock signal to every flip-flop at the same time. This results in predictable timing behaviour, lower propagation latency, and greater reliability, which makes synchronous counters the preferred choice in modern digital designs. A particular kind of counter that cycles through ten different states and usually represents decimal numbers from 0 to 9 is called a MOD-10 counter, sometimes known as a decade counter. After reaching the count of nine, the counter resets to zero and resumes the counting procedure. Digital clocks,

frequency counters, and display drivers are just a few of the many decimal counting applications that use MOD-10 counters. A minimum of four storage components (flip-flops or latches) are needed to create a MOD-10 counter since ten different states are needed, and four bits can represent up to sixteen states. The basic storage components of synchronous counters are flip-flops. Conventional edge-triggered flip-flops only sample input data when the clock signal is rising or falling. Even while edge-triggered flip-flops have distinct timing bounds, their constant clock flipping and greater clock loading frequently lead to higher clock power consumption. Furthermore, with deep submicron VLSI technologies, edge-triggered designs could be more vulnerable to tim in violations and clock skew. To overcome these issues, latch-based and dual-latch flip-flop systems have attracted substantial attention in recent years. A master (or sensing) latch and a slave (or latching) latch are the two level-sensitive latches that make up a dual-latch flip-flop. Relatively few research have examined the usage of dual-latch flip-flops in MOD-10 synchronous counter implementations, despite the literature proposing an umbero flow-power flip-flop designs. The design and modelling of a MOD-10 synchronous counter utilising dual-latch flip-flops are shown in this work. In comparison to traditional flip-flop-based counters, the suggested design seeks to accomplish dependable counting operations with enhanced synchronisation and decreased glitch occurrence. When the counter reaches the terminal count, it will reset synchronously after cycling through decimal states from 0 to 9. Reset circuitry integration, state transition logic creation, and functional verification via simulation are all part of a methodical design process.

LITERATURE SURVEY

[1]Teresa, V. V., et al. (2022)This work focuses on improving image compression and quality retrieval for hyperspectral brain tumor diagnosis. The authors use a Binary to Excess-1 Converter based Carry Select Adder (CSLA) combined with D-Latch architecture to reduce power consumption. The dual-latch approach helps in minimizing switching activity and improves speed. Although the design achieves high speed and low power, the increased number of functional blocks leads to higher hardware complexity, making the design less suitable for compact implementations. [2]Veeramsetty, M., et al. (2021)The authors propose a low-power dual edge triggered flip-flop (DETFF) using a dynamic signal-driven clock gating architecture. By capturing data on both rising and falling edges of the clock, the effective clock frequency is reduced, thereby lowering dynamic power. The design shows significant power savings, but it requires precise clock alignment, making it sensitive to clock skew and difficult to implement in large-scale systems. [3] Priya, S., et al. (2020)This paper presents a low-power flip-flop for memory circuits using a transmission gate latch with reduced transistor count. The reduced number of transistors results in area efficiency and lower power dissipation. However, due to fewer restoring paths, the design becomes highly sensitive to noise, especially under low-voltage conditions, which limits its robustness in practical memory applications. [4]Ahmed, R., et al. (2019) The authors introduce dual-edge triggered storage elements using a hybrid latch-based architecture optimized for low-voltage operation. The flip-flop performs well in sub-threshold and near-threshold voltages, making it suitable for energy-constrained systems. However, at higher operating frequencies, the internal latch timing fails to meet setup and hold constraints, causing unreliable operation. [5]Chen, L., et al. (2018) This work proposes an efficient CMOS flip-flop using conditional pre-charge logic to reduce unnecessary switching. By activating internal nodes only when data changes, switching power is minimized. While power reduction is significant, the pre-charged internal nodes can become unstable, especially during leakagedominated conditions, affecting long-term reliability. [6]Park, J., et al. (2018) A conditional capture flip-flop is presented where data capture occurs only when an actual transition is detected. This technique avoids redundant switching and saves power. However, the additional control logic increases the silicon area, making it less suitable for highly area-constrained designs such as dense memory arrays. [7] Lin, Y., et al. (2017) This paper introduces a high-performance, low-power DETFF using pass-transistor logic and reduced internal nodes. The minimized node capacitance improves speed and reduces dynamic power. Despite performance gains, leakage current remains high, particularly in deep submicron

technologies, limiting its low-power effectiveness during standby modes.

III PROPOSED SYSTEM

In order to achieve better timing performance, lower power consumption, and glitch-free operation, the proposed system provides the design and simulation of a MOD-10 synchronous counter built utilising dual latch flip-flops. This design specifically makes use of dual-latch flip-flop architecture, which consists of a detecting latch and a holding latch, in contrast to traditional synchronous counters that rely on typical edge triggered D flip-flops handled as black-box components. The system is appropriate for high-reliability digital applications because of its internal structure, which permits controlled data acquisition and steady output transitions. The MOD-10 counter is made to count in binary from 0000 (0) to 1001 (9) before synchronously resetting to 0000 on the subsequent clock pulse. A single clock signal powers every flip-flop in the system, guaranteeing true synchronous operation. During the clock's sensing phase, the dual-latch flip-flop samples the input data and moves it to the latching stage during the hold phase. This division lessens the possibility of problems during state transitions and mini misesracial conditions. Each flip-flop's next-state inputs are generated using combinational logic based on the counter's current state. Without causing asynchronous behaviour, the reset logic is meticulously crafted to identify the terminal count (binary 1010) and push the counter back to its starting position. The suggested approach avoids the metastability problems that are frequently connected with asynchronous resets and maintains consistent timing by incorporating the reset condition into the synchronous logic.

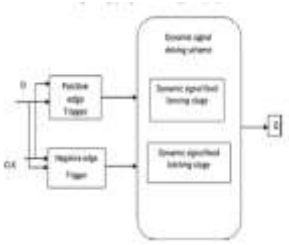


Fig 1. DSDS(DYNAMIC SIGNAL DRIVING SCHEME)

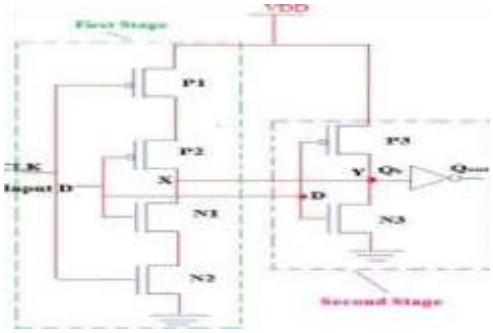


Fig 2. DSD-DETFF(DYNAMIC SIGNAL DRIVING- DUAL EDGE TRIGGER FLIP-FLOP)

The entire design is modelled using hardware description language (HDL) and simulated using industry standard simulation tools. Waveform analysis verifies synchronised output transitions, appropriate reset behaviour, and accurate counting operations. Because of controlled switching activity, the dual-latch technique exhibits lower clock skew sensitivity and better power efficiency as compared to conventional flip-flop-based devices.

All things considered, the suggested MOD-10 synchronous counter with dual-latch flip-flops offers a reliable and effective solution for digital counting applications. The design approach provides a scalable framework for low-power VLSI designs and higher-order counters while highlighting the benefits of latch based flip-flop implementation in synchronous systems.

MOD 10 SYNCHRONOUS COUNTER USINGD FLIP-FLOP

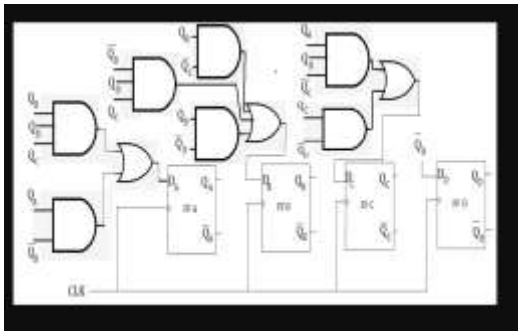


Fig 3. Mod-10 Synchronous Counter

The logic design of a MOD-10 synchronous counter constructed with D flip-flops and combinational logic is shown in the diagram, which can be realised using dual-latch flip-flop architecture. The counter is made up of four flip-flops with the labels FF A, FF B, FF C, and FF D. The outputs of these flip-flops are represented by the symbols Q A, Q B, Q C, and Q D.Q B Q C as well as Q D. Together, these four

outputs create a 4-bit binary value that indicates the counter's current count status. The next-state logic is determined by the combinational logic that comes before each flip-flop's D inputs. The present state outputs (QA, QB, QC, and QD) and their complements (QA, QB, QC, and QD) are taken as inputs by AND and OR gates.

This network's goal is to produce the appropriate D inputs (D A).D BD Cneeded to put into practice a MOD10countingsequence.The counter's least significant bit (LSB) is represented by flip-flop FF A. The reasoning behind feeding guarantees that, with the exception of the reset condition, Q A toggles on each clock pulse. The fundamental counting process is made possible by this behaviour. The OR gate that is attached to D AHigher-order bits of the counter are represented by flip-flops FF C and FF D. More intricate combinational logic that identifies particular count states powers their D inputs. When the counter reaches the decimal number 9 (binary 1001), it must reset, and this logic is crucial to MOD-10 operation. The logic synchronously pushes the subsequent state back to 0000 when the counter hits the invalid state (1010). The application of complemented outputs(Q)shows meticulous control over logic conditions, preventing errors and improper transitions. This strategy corresponds well with dual-latch flip-flop implementation, where data is first detected and then latched, ensuring reliable outputs throughout clock transitions. All things considered, the diagram shows a synchronous MOD-10 counter design that is well-organised. The system achieves dependable counting, less timing problems, and enhanced performance by fusing accurate next-state logic with synchronised clocking and latch-based flip-flop behaviour. For FPGA and VLSI applications where power efficiency and flawless operation are crucial, this design is ideal.

IV SIMULATION DIAGRAMS

A MOD-10 synchronous counter utilising D flip-flops is a sequential digital circuit that counts from 0 to 9 (decimal) in a synchronised manner and then resets to zero. The name MOD-10 denotes that the counter has ten unique states, while synchronous means that all flip-flops are driven by a common clock signal, assuring simultaneous state changes. Because of its straightforward input logic and dependable performance, D flipflops are frequently utilised in synchronous counters. Four D flip-flops are needed in a standard MOD-10 synchronous counter since $2^2 = 16$ states is enough to represent the ten necessary states (0000 to 1001). Reset logic is utilised to manage the remaining six unused states (1010 to 1111), which are regarded as invalid. One bit of the counter output, often denoted as Q_0 (LSB), Q_1, Q_2, and Q_3 (MSB), is stored in each D flip-flop. Four D flip-flop blocks connected in parallel to a single clock input typically make up the simulation diagram of the MOD-10 synchronous counter. Each flip-flop's D inputs are powered by combinational logic intended to generate the counter's subsequent state. State transition tables and Karnaugh maps are used to generate this logic, which minimises Boolean expressions. Since every flip-flop reacts to the clock edge simultaneously, there is no ripple delay, in contrast to asynchronous counters. The counter increases its value by one on each active clock edge during operation. The clock signal and the outputs Q_0, Q_1, Q_2, and Q_3 are usually displayed in the simulation waveform. Up to a count of nine, Q_0 toggles at every clock pulse, Q_1 every two pulses, Q_2 every four pulses, and Q_3 every eight pulses. The subsequent clock pulse initiates the reset condition when the output reaches 1001 (decimal 9).The simulation diagram has reset logic to guarantee correct MOD-10 behaviour. This code recognises the count 1010 (decimal 10) and quickly forces the counter back to 0000 An AND gate coupled to the Q_1 and Q_3 outputs can be used to execute the reset. All flip-flops can then receive an asynchronous or synchronous clear input. Timing reliability is increased in synchronous reset systems because the reset is triggered on the clock edge. The simulation results unequivocally show that the counter is operating correctly. The waveform displays a clear, flawless sequence from 0000 to 1001, then resets to 0000. The design is appropriate for high-speed digital systems because the counter is synchronous, meaning that all output transitions take place at the same moment. Simulation tools like as Model Sim, Vivado, Proteus, or Multisim are widely used to evaluate timing, logic correctness, and reset functionality.

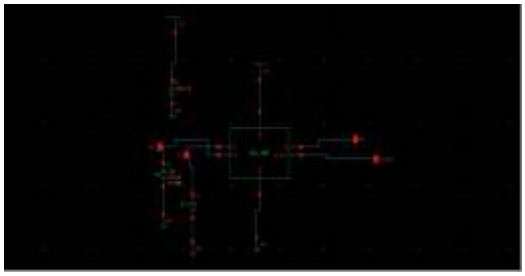


Fig 4. DSD-DETFF

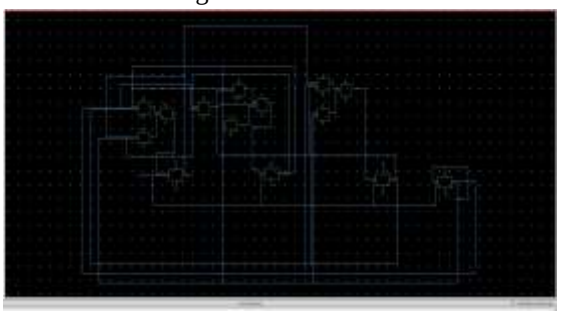


Fig 5. MOD-10 SYNCHRONOUS COUNTER

V RESULTS

Dual-latch flip-flops were used in the successful design and modelling of the MOD-10 synchronous counter. The counter achieves proper MOD-10 functionality by operating synchronously, counting from binary 0000 to 1001 and returning to 0000 upon the subsequent clock pulse. According to simulation results, ripple delay is eliminated and steady operation is ensured because all flip-flop outputs only transition on the active clock edge. Compared to traditional designs, the dual-latch flip-flop architecture offers glitch-free switching, enhanced timing control, and decreased propagation time. The reset logic precisely detects the terminal count and performs reliably without false triggering. Overall, the simulation shows that the suggested architecture is reliable, effective, and appropriate for FPGA or VLSI implementations and high-speed digital systems.

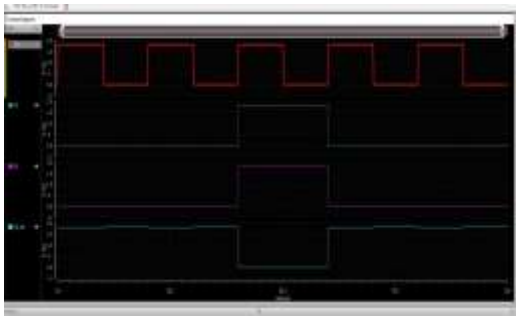


Fig 6.DSD-DETFF SIMULATION RESULT

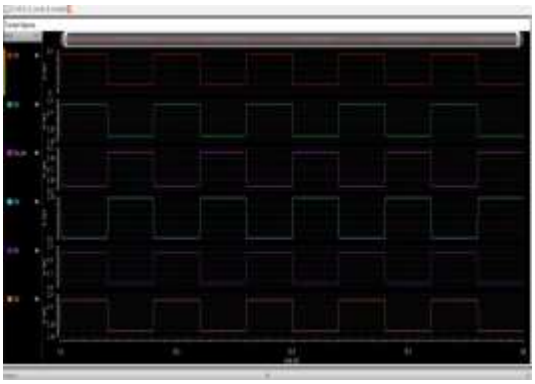


Fig 7. MOD-10 SYNCHRONOUS COUNTER RESULT

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Circuit inventory:
              nodes 45
            bsim3v3 86
            vsource 2
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Fig 8.Area

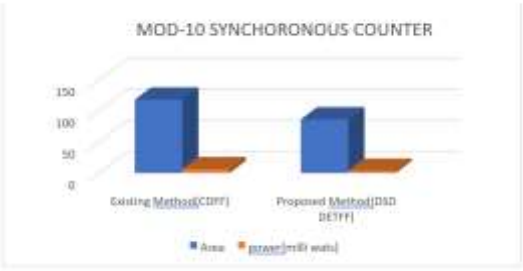


Fig 9.Comparison of CDFF and DSD DETFF

VI CONCLUSION

The design and simulation of a MOD-10 synchronous counter using dual-latch flip-flops has been successfully completed and verified. The counter operates with a common clock and counts from 0 to 9 in BCD format before resetting to zero, achieving MOD-10 operation. Dual-latch flip-flops improve timing reliability, ensure stable state transitions, and reduce race conditions compared to conventional flip-flops. Boolean expressions derived from the state transition table were implemented using basic logic gates, resulting in an efficient and compact circuit. Simulation results confirm correct counting sequences, proper reset operation, and glitch-free performance. The synchronous design eliminates ripple delays, providing improved speed and predictable timing, making the counter suitable for applications such as digital clocks, frequency dividers, and digital control systems.

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