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Research Paper

Design and Implementation of 15-Level & 25-Level Multilevel Inverter with Reduced Switching Count

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ABSTRACT: -In high and medium AC power applications, multilevel inverters (MLI) have significant importance in modern days. The architecture of multi-level inverter is preferred because of reduced harmonic distortion, high quality AC output power, least switching loss and minimum switching stress. The principal topology requires three dc voltage sources and ten changes to produce 15 levels over the heap. The augmentation of the main topology has been proposed as the subsequent topology, which comprises of four dc voltage sources and 12 changes to accomplish 25 levels at the yield. The DC supply for multilevel inverter is taken from solar panel with MPPT technique. The new multilevel inverter circuit topology, switching pattern and gate pulse making is explained in this paper. The Fast Fourier Transform (FFT) analysis of the outputs of 15-level and 25-level of multilevel inverters are shown in below. The new 12-switch 25 multilevel inverter circuit has been intended and modeled by using MATLAB software Simulink tool. The simulation results are displayed with less total harmonic distortion and reduced switching loss has been achieved.

Keywords: Multilevel Inverter (MLI), pulse width Modulation (PWM), power electronics, single-phase inverter, reduce switch count, Total harmonic distortion (THD).

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I. INTRODUCTION

Now a day, a huge number of industrialized applications have begun to demand high and medium power electronic appliances. On the other hand, power electronic switching devices are undergoing the medium voltage applications haven't created still now. The ever-expanding vitality utilization, petroleum derivatives' taking off expenses and modest nature, and compounding worldwide condition have made a blasting enthusiasm for sustainable power source age

frameworks, one of which is photovoltaic. Such a framework creates power by changing over the Sun's vitality straightforwardly into power. Photovoltaic-produced vitality can be conveyed to control framework systems through lattice associated inverters. A solitary stage network associated inverter is normally utilized for private or low-power utilizations of intensity extends that are under 10 Kw.

Staggered inverters are promising; they have almost sinusoidal yield voltage waveforms,

yield current with better symphonious profile, less worrying of electronic parts attributable to diminished voltages, exchanging misfortunes that are lower than those of regular inverters. The MLI technology not simply generates higher voltage levels, other than promotes renewable power generation devices in input side. MLI (Multi level inverter) is one of the electrical power conversion strategies that produce AC type voltage as output side using input DC source. Various topologies for multilevel inverters have been proposed over the years. Common ones are Unbiased Point Clamped (NPC), Flying Capacitor (FC) and Cascade H-Bridge (CHB). , MLI discover their applications in pretty much every field of electrical building including sustainable power source frameworks, HVDC applications, disseminated age (DG) framework, mechanical drive applications, uninterruptible force supplies, etc. They are widely used in drives and other allied areas in industries. In spite of the fact that there are hardly any issues with the regular MLI like a higher number of source prerequisite, voltage adjusting of the capacitor and huge switch necessity in CHB geography, FC geography and NPC geography separately.

In light of this, MLIs have been delegated even and unbalanced. Balanced MLIs utilizes indistinguishable dc voltage sources while topsy-turvy MLIs utilizes dc voltage sources having inconsistent extent. Balanced MLIs have increasingly repetitive states for example progressively number of exchanging mix are accessible to get same voltage level. This improves the presentation of MLI as far as adjusting the voltage across capacitors and shortcoming open minded abilities. In any case, simultaneously even designed MLIs requires progressively number of switches, entryway driver

circuits, and dc voltage joins. This expands the inverter size, cost and control unpredictability for a higher number of levels. Uneven arrangement builds the quantity of levels produced at the yield looks at to the even setup utilizing a similar number of parts and dc voltage sources. The topology was applied to a grid-connected photovoltaic system with considerations for a maximum-power-point tracker (MPPT) control algorithm.

In this paper, work has been carried out with the aim of reducing the number of power semiconductor devices and dc voltage sources, while achieving a higher number of levels at the same time. This paper is organized as follows: Section II describes the proposed topology with its extension for a higher number of level. To set the benchmark of the proposed method, Section III gives a quantitative examination of the proposed geographies utilizing a similar number of switches. Segment IV expounds the different simulation results and Section V summarizes the paper.

II. PROPOSED MULTILEVEL INVERTER

A. PROPOSED THREE SOURCE 15 LEVEL TOPOLOGY

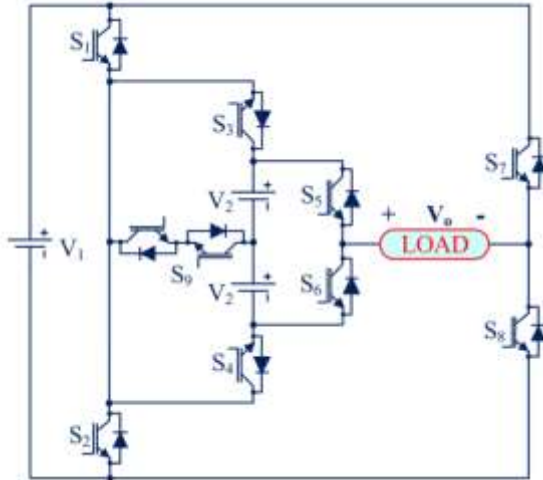


Fig. 1. Proposed 3S-15L topology.

The proposed topology is shown in Fig. 1. It consists of eight unidirectional switches from S1 - S8 along with one bidirectional switch S9. The switches S3 - S6 along with S9 forms the inner part of the topology with two dc voltage sources with a magnitude of V2.

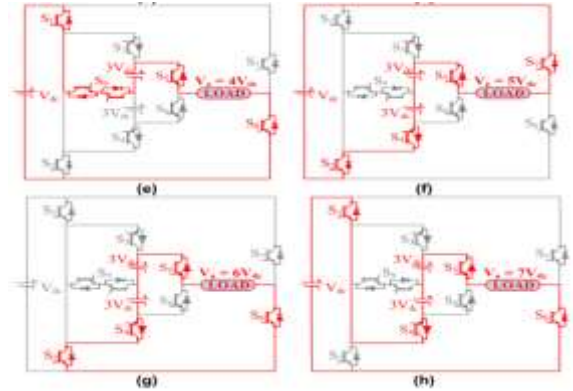
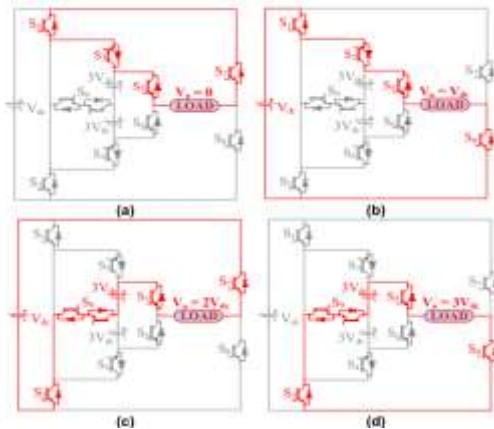


Fig 2. Different switching states of the proposed 3S-15L topology in positive half cycle. (a) $V_o = 0$. (b) $V_o = V_{dc}$. (c) $V_o = 2V_{dc}$. (d) $V_o = 3V_{dc}$. (e) $V_o = 4V_{dc}$. (f) $V_o = 5V_{dc}$. (g) $V_o = 6V_{dc}$. (h) $V_o = 7V_{dc}$.

The remaining four switches i.e., S1 – S2 and S7 – S8 and one dc voltage source with magnitude of V1 forms the outer portion of the proposed topology. The switches (S1–S2), (S3–S4), (S5–S6), and (S7–S8) need to operate in a complementary fashion to avoid short-circuiting of dc voltage sources. The number of levels depends upon the magnitude of the dc voltage source, i.e., V1 and V2 the selection can be done in two ways as:

1) SYMMETRICAL CONFIGURATION :

In this configuration, each dc voltage source has the same magnitude, i.e., $V_1 = V_2 = V_{dc}$. With such configuration, seven levels at the output are achieved.

2) ASYMMETRICAL CONFIGURATION :

In the asymmetrical configuration, the magnitude of dc voltage sources have different magnitude, i.e., V1 and V2 have a different magnitude. For the

proposed topology with asymmetrical configuration, the magnitude of dc voltage sources are chosen in tertiary mode, i.e., $V1 = V_{dc}$, and $V2 = 3V_{dc}$ (3S-15L Topology). With the tertiary configuration, the proposed topology generates 15 output voltage levels, i.e., zero, $\pm V_{dc}$, $\pm 2V_{dc}$, $\pm 3V_{dc}$, $\pm 4V_{dc}$, $\pm 5V_{dc}$, $\pm 6V_{dc}$, and $\pm 7V_{dc}$. The switching table for the proposed topology with the tertiary mode is given in Table 1. Furthermore, the different switching states for the proposed topology with tertiary mode are shown in Figs. 2 (a)-(h).

TABLE 1. Switching state for the proposed 3S-15L topology.

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	V_o
1	0	0	1	1	0	0	1	0	$7V_{dc}$
0	1	0	1	1	0	0	1	0	$6V_{dc}$
0	1	0	1	1	0	1	0	0	$5V_{dc}$
1	0	0	0	1	0	0	1	1	$4V_{dc}$
0	1	0	0	1	0	0	1	1	$3V_{dc}$
0	1	0	0	1	0	1	0	1	$2V_{dc}$
1	0	1	0	1	0	0	1	0	V_{dc}
1	0	1	0	1	0	1	0	0	0
0	1	0	1	0	1	1	0	0	$-V_{dc}$
1	0	0	0	0	1	0	1	1	$-2V_{dc}$
1	0	0	0	0	1	1	0	1	$-3V_{dc}$
0	1	0	0	0	1	1	0	1	$-4V_{dc}$
1	0	1	0	0	1	0	1	0	$-5V_{dc}$
1	0	1	0	0	1	1	0	0	$-6V_{dc}$
0	1	1	0	0	1	1	0	0	$-7V_{dc}$

B. PROPOSED FOUR SOURCE 25 LEVEL (4S-25L) TOPOLOGY

The proposed 3S-15L topology can be extended by replacing the single dc voltage source of magnitude $V1$ with a T-configured two dc voltage sources with same magnitude $V1$ as shown in Fig. 3. With the addition of one dc voltage source with magnitude $V1$ and a bidirectional switch S_{10} , there is an addition in the number of levels. Again, for the symmetrical configuration, the proposed topology can generate nine levels. However, for asymmetrical configuration,

the number of levels increases to 25. The 25 level output is achieved by selecting $V1 = V_{dc}$ and $V2 = 5V_{dc}$. The different switching combination for the proposed topology with four dc voltage sources generating 25 levels is given in Table 2.

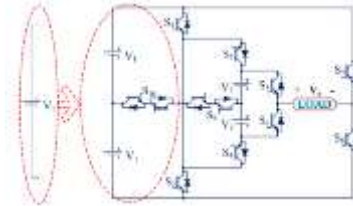


Fig 3. Proposed 4S-25L topology.

TABLE 2. Switching state for the proposed 4S-25L topology.

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	V_o
1	0	0	1	1	0	0	1	0	0	$12V_{dc}$
0	0	0	1	1	0	0	1	0	1	$11V_{dc}$
1	0	0	1	1	0	1	0	0	0	$10V_{dc}$
0	0	0	1	1	0	1	0	0	1	$9V_{dc}$
0	1	0	1	1	0	1	0	0	0	$8V_{dc}$
1	0	0	0	1	0	0	1	1	0	$7V_{dc}$
0	0	0	0	1	0	0	1	1	1	$6V_{dc}$
1	0	0	0	1	0	1	0	1	0	$5V_{dc}$
0	0	0	0	1	0	1	0	1	1	$4V_{dc}$
0	1	0	0	1	0	1	0	1	0	$3V_{dc}$
1	0	1	0	1	0	0	1	0	0	$2V_{dc}$
0	0	1	0	1	0	0	1	0	1	V_{dc}
1	0	1	0	1	0	1	0	0	0	0
0	0	0	1	0	1	0	1	0	1	$-V_{dc}$
0	1	0	1	0	1	1	0	0	0	$-2V_{dc}$
1	0	0	0	0	1	0	1	1	0	$-3V_{dc}$
0	0	0	0	0	1	0	1	1	1	$-4V_{dc}$
0	1	0	0	0	1	0	1	1	0	$-5V_{dc}$
0	0	0	0	0	1	1	0	1	1	$-6V_{dc}$
0	1	0	0	0	1	1	0	1	0	$-7V_{dc}$
1	0	1	0	0	1	0	1	0	0	$-8V_{dc}$
0	0	1	0	0	1	0	1	0	1	$-9V_{dc}$
0	1	1	0	0	1	0	1	0	0	$-10V_{dc}$
0	0	1	0	0	1	1	0	0	1	$-11V_{dc}$
0	1	1	0	0	1	0	1	0	0	$-12V_{dc}$

III. NEW 25-LEVEL 12-SWITCH MLI – PV panel supply:

The new 25-level MLI circuit contains 12-switching devices and 3-DC supply source. The conventional 11-level multilevel inverter used 8-switches and 3-DC source. Compared to conventional technique, the proposed technique generates 4-more levels by using 12-switches. Figure 4 shows the block diagram of proposed 25-level MLI.

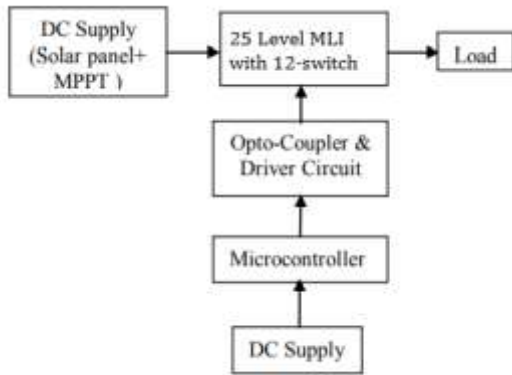


Fig. 4 Proposed block diagram

The components present in this proposed method are solar panel, 15-level multilevel inverter, AC load, microcontroller, opto-coupler and driver circuit. Each and every unit is explained in below sections.

a. SOLAR CELL AND PANEL MODELLING

Design and modeling of photovoltaic cell and panel can be derived by many methods in software like PSPICE & MATLAB etc. There are numerous schemes to symbolize a model as like Physical modeling, Mathematical modeling and Embedded Programming.

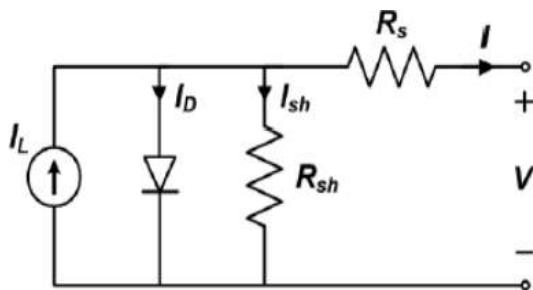


Fig. 5 Electrical equivalent of photovoltaic cell

Electrical equivalent circuit of single photovoltaic cell is displayed in figure 5. In the circuit diagram R_s indicates series resistance of P-N junction of solar cell and

R_{sh} indicates shunt resistance. The voltage-current characteristics of solar cell depend upon series resistor. I_D is current flows through diode and I_{sh} is shunt leakage current. The output current I is calculated by applying KCL in equivalent circuit:

$$I = I_{PH} - (I_D + I_{SH})$$

From the equivalent circuit, output current is the sum of diode current and shunt resistor current. Hence the simplified equation is

$$I = I_{PH} - I_O$$

Photon current (I_{ph}) is produced on incorporation of solar irradiation by photovoltaic cell therefore photocurrent (I_{ph}) value is directly linked to deviation in solar temperature and irradiance that is

$$I_{PH} = (I_{SCR} + K_I \Delta T) \frac{G}{G_R}$$

The photovoltaic cell reverse saturation current (I_{rs}) will be determined by

$$I_O = I_{rs} \left(\frac{T}{T_{ref}} \right)^3 \exp \left[\left(\frac{q E_{go}}{AK} \right) \left(\frac{\Delta T}{T_{ref} T} \right) \right]$$

Where,

I_{rs} - reverse saturation current.

E_{go} - band-gap energy of pn junction material.

The current values of I_o and I_{ph} will derived the value of current I as follows

$$I_{PV} = I_{ph} - I_O \left[\exp \left(\frac{q (V_{PV} + I_{PV} R_S)}{AKT} \right) - 1 \right] - \frac{(V_{PV} + I_{PV} R_S)}{R_P}$$

The power output is exaggerated by weather constraint variations that are shading and temperature.

b. MPPT BY P&O TECHNIQUE

Power generation of solar panel depends upon climatic condition such as temperature and radiation. MPPT (Maximum Power Point Tracking) method is a technique used to regulate output DC voltage of solar panel. Perturb and observation algorithm is used to MPPT technique. Figure 6 displays flow chart of P&O. This algorithm senses the input voltage and current from photovoltaic panel using voltage and current sensors.

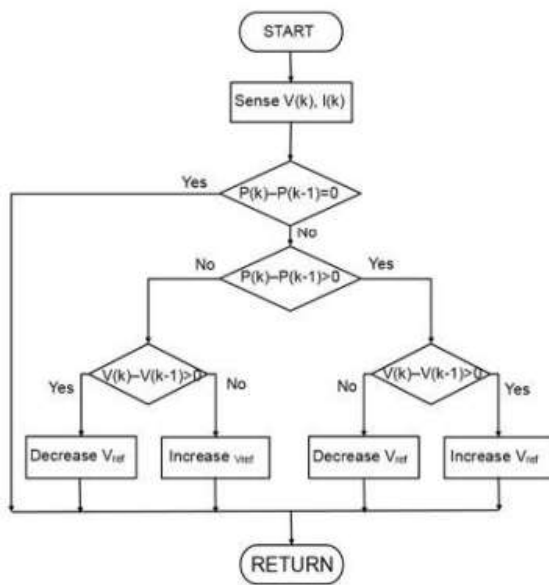


Fig. 6 Flowchart for P&O algorithm

IV. SIMULATION RESULT:

The working of new 25-level circuit is analyzed by MATLAB software. Simulation circuit, gate pulse, output voltage, output current and THD waveforms are explained in this section.

SIMULATION CIRCUIT DIAGRAM OF PROPOSED MLI:

Figure.7& 9 demonstrates the 15-level&25-level MLI circuit diagram drawn in MATLAB Simulink software. Gate pulses

are given to all controlled switching devices and resistive load is used to measure AC output voltage. Voltage and current measurement blocks are used to display output AC voltage and current. FFT analysis block is present in MATLAB to measure THD present in AC voltage.

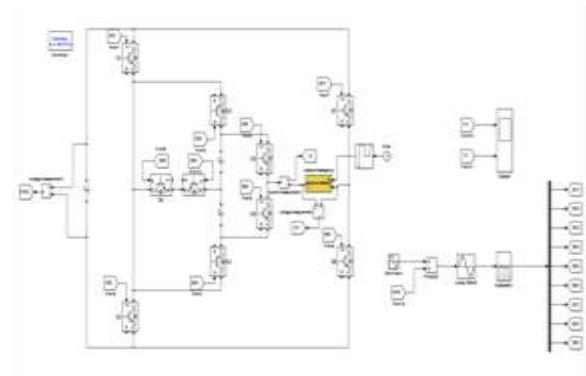


Fig. 7 Simulation circuit diagram of 15-level MLI(R LOAD)

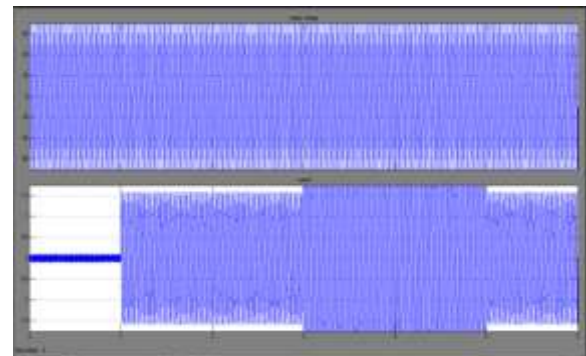


Fig 8. Simulation results for 15 levels output (a) output voltage and current waveform with different resistive load [scale: vo = 40V/div, io =2A/div]

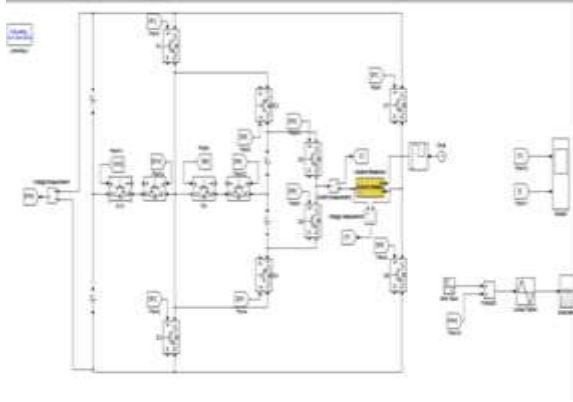


Fig. 9. Simulation circuit diagram of 15-level MLI (RL LOAD)

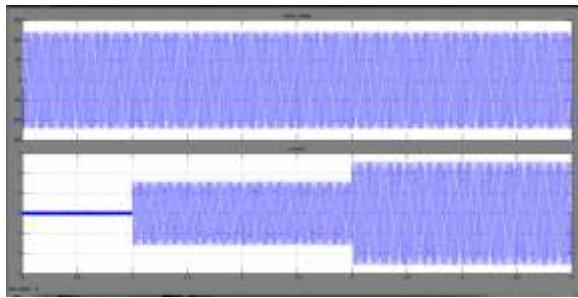


Fig 10. Simulation results for 15 levels output (a) output voltage and current waveform with different resistive-inductive load [scale: $v_o = 40V/div$, $i_o = 2A/div$].

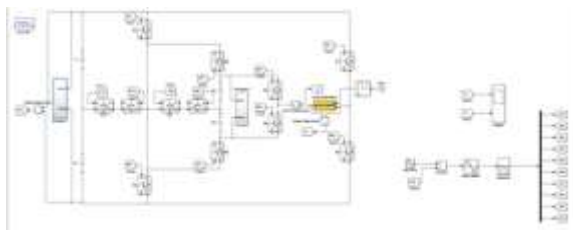


Fig. 11. Simulation circuit diagram of 25-level MLI connected to pv panel (RL LOAD)

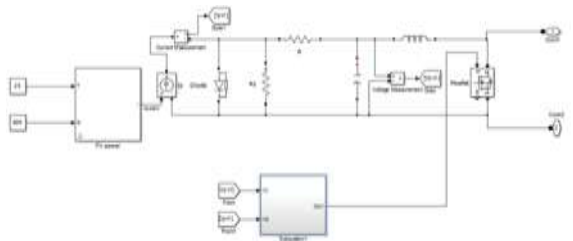


Fig.12. SOLAR PANEL (PV)

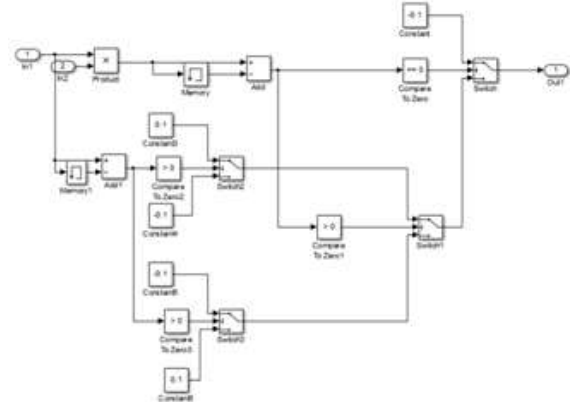


Fig 13. P&O (Perturb and observe) method

Output Results:

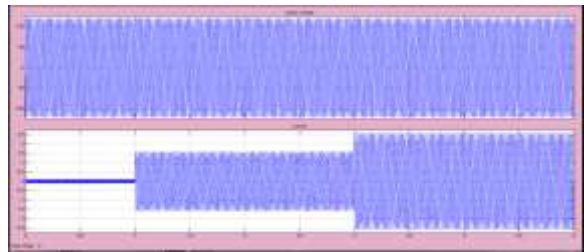
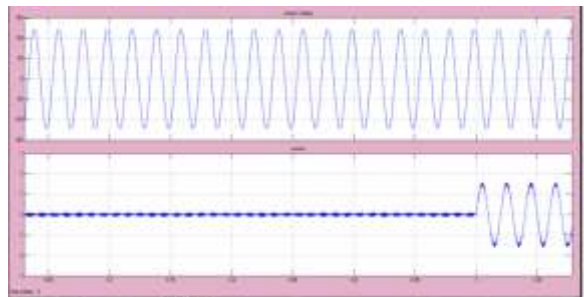
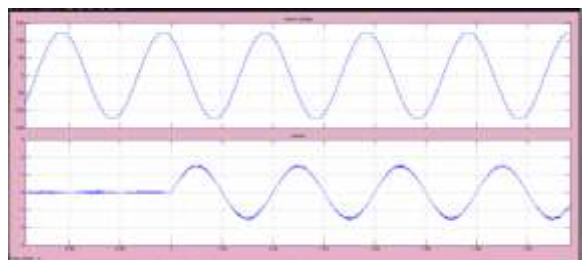


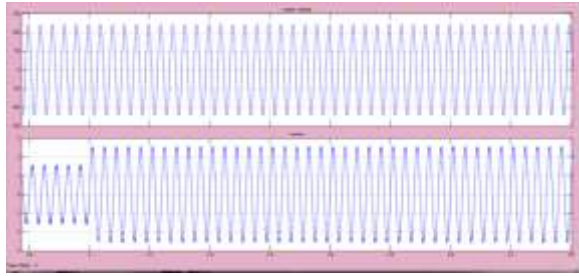
Fig 10. Simulation results for 25 levels output (a) output voltage and current waveform with different resistive-inductive load [scale: $v_o = 40V/div$, $i_o = 2A/div$].



(b) transient-state waveforms with change of load from $R=0$ to $R=100 \Omega$ [scale: $v_o = 100V/div$, $i_o = 2A/div$]



(c) transient-state waveforms with change of load from Z=0 to Z=60 \square + 100 mH.



(d) transient-state waveforms with change of load from R=100 \square to R=50 , [scale: vo = 40V/div, io =2A/div].

I. THD (HARMONIC DISTORTION):

THD is a computation of nearness value to waveform which is attain to the outline of the fundamental frequency waveform. It can be determined by using following equation

$$THD = \frac{1}{V_1} \sqrt{\sum_{n=2,3}^{\infty} V_n^2}$$

Where, V1-Voltage with fundamental frequency and Vn-Voltage of nth order frequency wave.

THD ANALYSIS OF 15-LEVEL MLI:

The THD analysis of 15-level multilevel inverter with 8-switching device is shown in figure 11. The total harmonic distortion resnet in this waveform is around 9%.

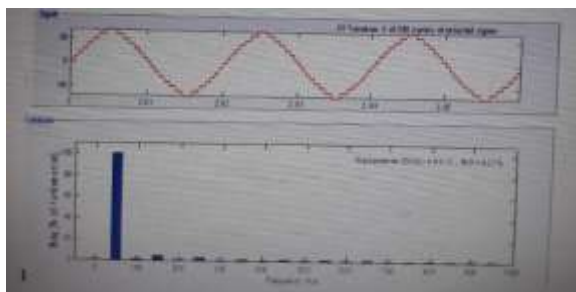


Fig 11: THD analysis of 15-level MLI

THD ANALYSIS OF 25-LEVEL MLI WITH PV PANEL SUPPLY:

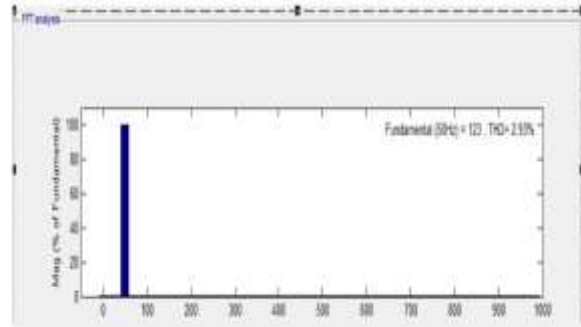


Fig 12: The THD analysis of 25-level multilevel inverter with PV panel

The THD analysis of 25-level multilevel inverter with PV panel supply 12-switching device is shown in figure 12. The total harmonic distortion resnet in this waveform is around 3%.

In figure the AC voltage is taken as input parameter for FFT analysis is done using the given sampling time, samples per second etc through which total harmonic distortion can be calculated.

V. CONCLUSION

The proposed method has been examined in subtleties with the fundamental unit with 3S-15L arrangement creating 15 levels, and the augmentation of the proposed geography with 4S-25L setup to accomplish 25 levels. Thus a new 25 level inverter connected to PV panel

Single phase AC voltage topology has been proposed with 12 power semiconductor switching device, less THD and low conduction loss and switching stress and loss. In consequence of using less switching devices, automatically reduce the circuit complexity, size and cost, which automatically decrease the conduction and switching and losses. The main advantage of this proposed method rather than existing scheme is huge drop of THD. The

circuit configuration of proposed method is simple hence the gate pulse making and control strategy also very simple. The harmonic distortion of proposed 25-level AC output voltage has been reduced around 2% when compared to conventional inverters. At last, a few recreation results demonstrates the reasonableness and functionality of the proposed method with various sort of stacking mixes considering the difference in balance lists .These results are obtained from the simulation of MATLAB Simulink software.

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