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Research Paper

DESIGN AND ANALYSIS OF LOW-POWER, HIGH-SPEEDERROR-TOLERANTADDERUSING GATEDIFFUSIONINPUTTECHNIQUE

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ABSTRACT

Instate-of-the-artVLSIcircuits,completelypreciseresultsarenotalwaysessential.Asaresult, engineershavebeguntodeveloperror-tolerantcircuitsthatprovidesatisfactoryperformancefor computing tasks. Building on this concept, the Error Tolerant Adder (ETA) emerges as a promisingsolution,offeringamethodforachievingexcellentpowerandspeedperformance.This paperpresentsa32-bitETAdesignedusingtheGateDiffusion Input(GDI)technique,amodern and efficient logic design style. The proposed design features an 11transistor (11T) GDI full adder,whichsignificantlyreducestheareaintermsoftransistorcountwhilealsoenhancingdelay andpowerperformance.Accordingtosimulationdata,theproposeddesignsurpassestheexisting designsintermsofthePowerandDelay.TheadoptionoftheGDItechniqueallowsforminimized power consumption and improved processing speed, making it a highly efficient choice for contemporary VLSI circuit design. This approach demonstrates how error-tolerant computing can be effectively implemented to meet the demanding requirements of modern electronic systems, where performance and energy efficiency are paramount.

The need for low power portable devices has increased due to the expanding market for multimedia applications. High speed performance is also preferred at the same time. Designers have begun to compromise on accuracy in order to concurrently accomplish both of these objectives. Speed and power consumption have improved byimplementing this novel idea. The traditional CMOS logic style has been used to construct the ETA design. The hardware implementation of our suggested architecture uses the gate diffusion input (GDI) approach. A brand-new type of logic design known as GDI reduces the transistor count significantly. By adoptingthis technique, simplelogicoperations that call forfour, six, oreven twelvetransistors in typical CMOS logic style can be created with just two transistors.

ThetoolsusedintheprojectareS-Edit,T-SpiceandW-Edit,whicharepopularsimulation tools used for simulating electronic circuits. The GDI technique is used to reduce power consumptionandincreasespeed.Theproposedadderiscomparedwithexistingaddersinterms of power consumption, speed, and error tolerance. The results show that the proposed adder achieves high-speed performance, low power consumption, and error tolerance. The proposed adder is suitable for various applications, including digital signal processing, arithmetic logic units, and low-power electronics. The hardware implementation of our suggested architecture uses the gate diffusion input (GDI) approach.Abrand-new type of logic design known as GDI reduces the transistor count significantly. By adopting this technique.

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INTRODUCTION

The increasing demand for high-performance and low-power digital circuits has led to the development of innovative design techniques. One such technique is the Gate Diffusion Input (GDI)method,whichhasbeenwidelyusedtodesignhi

gh-speedandlow-powerdigitalcircuits. In this context, this project focuses on designing a high-speed, low-power, and error-tolerant adder using the GDI technique.

IndigitalVLSIcircuits,perfectlyaccurateoutputsare notalwaysneeded.Sodesignershave started to design error tolerance circuits which provide good enough output for computation. Onthebasisofthisfact,errortolerantadder(ETA)isde signedwhichprovidesawaytoachieve goodpowerandspeedperformance.Inthispaper,ane merginglogicstyleofcircuitdesign,gate diffusion input (GDI) technique is adopted to design a 32-bit ETA.

The proposed design reduces area in terms of area the transistor count to a great extent as well as improves the delay and power performance. Simulation results have shown that proposed design achieves 38% improvement in the Power-Delay-Product when compared to the existing design.

Adders are fundamental components in digital circuits, and their performance has a significantimpactontheoverallsystem.Addersareus edtoperformarithmeticoperations,such as addition and subtraction, in digital systems. In this report, we will provide a detailed description of adders, including their types, design considerations, applications, and design techniques.

OBJECTIVE

This reality incited the improvement of the Slip-up Merciful Snake, a thought of bungle versatility used essentially in adders (assessed season of appearance). As a result of the time expected for convey causing beginning with one stage then onto the following, which achieves the languid working speed of customary adders, assessed season of appearance was made to dispose of the necessity for convey spread similarly movement. Speed and power use have improved by executing this unique idea.

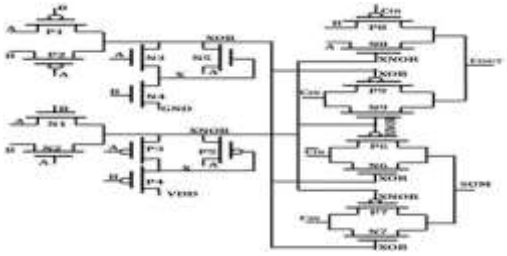
However, implementing GDI-based error-tolerant adders is not without challenges. The unique biasing requirements of GDI gates may complicate integration with standard CMOS logic, particularly in mixed-signal environments. Moreover, ensuring signal integrity and avoiding logic level degradation require careful circuit-level design and simulation. Nevertheless, these challenges are increasingly being addressed through refined GDI cell librariesandimprovedelectronicdesignautomation(E DA)toolsthatsupportmixed-logicdesign flows. Additionally, with the increasing acceptance of approximate and inexact computing principles in mainstream applications, the slight compromises inherent in errortolerant adders are becoming more acceptable, even in high-performance systems.

In summary, the combination of the GDI technique with the principles of error-tolerant design represents a highly promising approach for constructing high-speed adders tailored to moderncomputationalneeds.Byreducingthetransisto rcountandoptimizingsignalpropagation paths,GDI-basedlogicsignificantlyenhancesthespeedandenergy efficiencyofaddercircuits. When these benefits are coupled with an architecture that tolerates minor computational errors, theresultisanarithmeticunitthatmeetsthestringentde mandsofcontemporaryandfuture digital systems. This synergy of design philosophies not only enables efficient hardware implementations but also opens up new avenues in energy-aware and approximate computing.

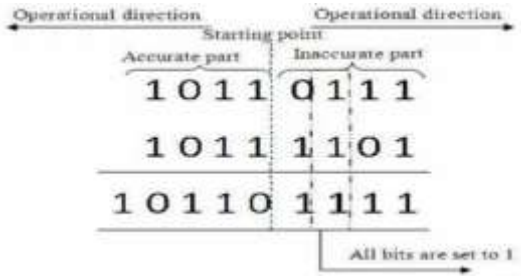
As the industry continues to push toward higher performance with lower power budgets and greater computational complexity, innovations like high-speed error-tolerant adders using GDI logic are likely to become central to the evolution of digital circuit design.

PROPOSED SYSTEMS

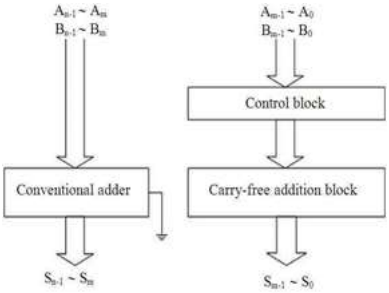
Adders are fundamental components in digital circuits, and their performance has a significant impactontheoverallsystem.Traditionaladderdesigns oftencompromisebetweenspeed,power consumption, and error tolerance. The GDI technique offers a promising solution to achieve a balance between these competing factors.



Circuitdiagramofproposedsystem



AccuratepartandInaccuratepartbits



ErrorTolerantAdder(ETA)

There is a huge improvement in the power and speed when we use an ETA. For increasing the speed and decreasing the power dissipation, we use the logic that in an adder circuit the delay appears mainlybecause of the carrypropagation and also there is a lot of power dissipation

BasicoperationofETA

In the basic structure of ETA, the operands are divided into two parts: accurate and inaccurate one.The length of each part can be equal or unequal depending on the requirement of accuracy and speed.We are considering 12 bits in accurate part and remaining 20 bits in inaccurate part.

Theadditionprocessstartsfromthejoiningpointoftwopart sandgoestowardsthetwoopposite directions simultaneously.

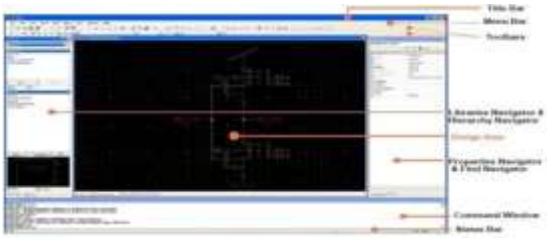
Thecontrolblockchecksallthebitsfedtotheinaccurate partandmonitorswhenbothincoming bits go high

Basic Block Diagram of ETA

Theaccuratepartcanbedesignedbyusinganyoneofthe availabletraditionaladderslikeripple carryadder, carrylook ahead adder, carrybypass adder and etc.Theinaccuratepartis designed such as to eliminate the propagation of carryfrom one bit to next one.Thispart consists of two blocks:controlblockandcarryfreeadditionblock..The controlblockoutputatthatpositionand that to the right of that position are then made high.

DESIGN APPROACHES

The user interface consists of the elements shown below. Unless you explicitly retrieve a setup file, the position, docking status and other display characteristics are saved with a design and will be restored when the design is loaded.



ElementsintheS-EditTool

PartsoftheUserInterfaceTitleBar

Thetitlebarshowsthenameofthecurrentcellandtheviewt ype(symbol,schematic, etc.).

MenuBar

The menu bar contains the S-Edit menu titles. The menu displayed may vary depending on the viewtypethatisactive.See“ShortcutsforCellandView Commands”onpage70forthevarious methods S-Edit provides for executing commands.

MenuListFiltering

Most S-Edit menus and dialogs allow for filtering to speed the process of selecting from a dropdown list. So, when you enter a character, S-Edit will jump to the first list item that begins withthatcharacter.

Toolbars

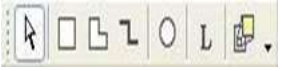
You can display or hide individual toolbars using the **View > Toolbars** command, or by rightclickinginthetoolbarregion.Toolbarscanbereloc atedanddocked as youlike. Foradded convenience, S-Edit displays a tool tip when the cursor hovers over an icon.

StandardToolbar

TheStandardtoolbarprovidesbuttonsforcommonlyused fileandeditingcommands,aswellas operations specific to S-Edit such as “View Symbol.”

DrawToolbar

TheDrawtoolbarprovidestoolsusedtocreatenon-electricalobjects,suchasrectangles,circles, and lines, for illustrating and documenting a design.



SegmentToolbar

TheSegmenttoolbarprovidestoolswithwhichyoulimitth edegreeofangularfreedomallowed when you are drawing wires.

ElectricalToolbar

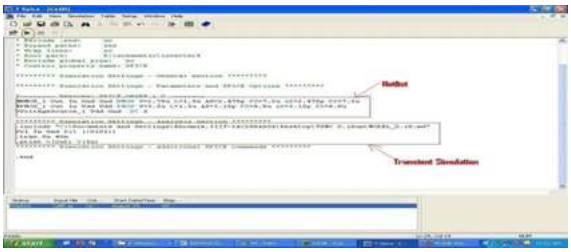
TheElectricaltoolbarprovidesthetoolsusedtocreatewires,nets,andports,andtoadd properties.

SPICESimulationToolbar

TheSPICESimulationtoolbarletsyouextractconnectivity,selectandprobenets,launchTSpice and select evaluated properties.

Simulationtool

Thetoolusedforsimulationpurposefort heentireresearchworkisTannerEDA tool version 13.0.Thefeaturesandfunctionalityofthistoolhasbeendescribedbelow:



SIMULATIONTOOL

Thedesigncycleforthedevelopmentofelectroniccircuitsincludesanimportantprefabrication verification phase. Because of the expense and time pressures associated with the fabrication step, accurate verification is crucial to efficient design. The role of EDAtool is to help design andverifyacircuit'soperationbynumericallysolvingthedifferentialequationsdescribingthe circuit. These simulation results allow circuit designers to verify and fine-tune designs before submittingthemforfabrication.TannerEDAtoolisacompletecircuitdesignandanalysissystem that includes

T-SPICE

Totransformyourideasintodesigns,youmustbeable tosimulatelargecircuitsquicklyandwith a high degree of accuracy. That means you need a simulation tool that offers fast run times, integrateswith yourotherdesigntools,andiscompatiblewith industrystandards.TannerT-Spice Circuit Simulator puts you in control of simulation jobs with an easy-to-use graphical interface and a faster, more intuitive design environment.

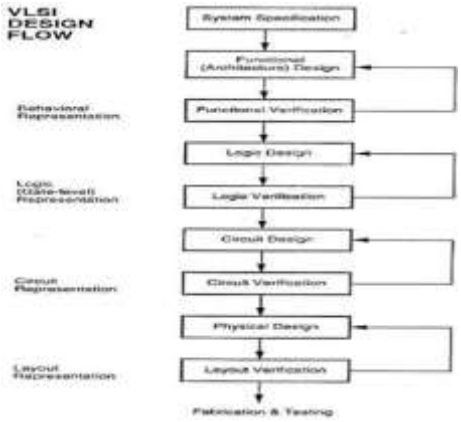
Speed**:** T-Spice provides highly optimized code for evaluating device models formulatingthesystemsoflinearequations,andsolvingthosesystems

- **Convergence:**T-Spiceusesadvancedmathematicalmethodsto achievesuperior numericalstability.Largecircuitsandfeedbackcircuits,impossibletoanalyzewithother SPICE products, can be simulated in T-Spice.
- **Accuracy**: T-Spice uses very accurate numerical methods and charge conservation to achieve superior simulation accuracy.
- **Macro modeling**:T-Spice simulates circuits containing "black box" macro devices.A macro device can directly use experimental data as its device model. Macro devices can also represent complex devices, such as logic gates, for which only the overall transfer characteristics, are of interest.

WORKING

Digital systems are highly complex at their most detailed level. They may consist of millions of elements i.e., transistors or logic gates. For many decades, logic schematics served as then GurFrancaoflogicdesign,butnotanymore.Today,hardwarecomplexityhasgrowntosucha degreethataschematicwithlogicgatesisalmostusele ssasitshowsonlyawebofconnectivity and not functionality of design. Since the 1970s, computer engineers, electrical engineers and electronics engineers have moved toward Hardware description language (HDLs).

VLSI Designflow



TypicaldesignflowfordesigningVLSIcircuitsisshowninthetoolflowdiagram.Thisdesign flow is typically used by designers who use HDLs. In any design,

specification is first. Specification describes the functionality, interface and overall architecture of the digital circuit to be designed. At this point, architects need not think about how they will implement their circuit.Abehavioral description is then created to analyze the design in terms of functionality, performances and other high level issues. The behavioral description is manually converted to an RTL(RegisterTransfer Level) description in an HDL.The designer has to describe the data flowthatwillimplementthedesireddigitalcircuit.Fro mthispointonwardthedesignprocessis done with assistance of CAD tools.

DesignSpecification

- TheprojectSpecificationsandrequirementsare writtenfirst
- Thedigital circuit functionalityisexplained forthearchitectureto be designed.
- Specification:Ituseswaveformer,testbencheror wordfordrawingwaveform.

RTLDescription

CADToolsareusedforcodingformatfortheConversation ofSpecification.

Coding Styles:

- GateLevel Modeling
- DataFlowModeling
- BehavioralModeling

Logic Synthesis

- RTLdescriptionintoGatelevel-Netlistform conservation.
- Thecircuitisdescribedasafunctionofgates andconnections.
- Synthesis: Synthesis is done byAltera and Xilinx, Simplify Pro, Leonardo Spectrum Design Compiler, FPGA Compiler.

Implementation

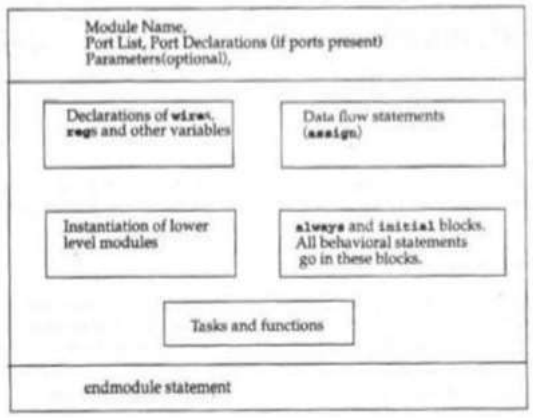
- Thedesignprocessisthefinalstagein implementation.
- CodingandRTLcanbeimplementedusingIntegra ted circuits.

Modules

Distinct parts of a Verilog module consists of are as shown in below figure. The keyword moduleisthebeginningofamoduledefinition. Inamoduledefinitionthemodulename,port list, port declarations, and optional parameters must come first in its definition. If the module hasanyportstointeractwiththeexternalenviron mentthenonlyPortlistandport declarations are present. There are five components within a module

- variabledeclarations,
- dataflowstatements
- instantiationoflower modules
- behaviouralblocks
- task orfunctions.

Module design



Module design

Example:

ModuleStructure:

module<modulename>(<module_terminals_list>); …..<moduleinternals>…. Endmodule

Ports

The interface between a module and its environment is provided by the ports. The input/output pins of an Integrated Circuit chip are its ports. The environment cannot see the internals of the module. It is a great advantage for the designer. As long as the interface is not modified the internals of the module may be mod ifiedwithout affecting its environment.Terminals are the synonyms for the ports.

Port Declaration

Themodulemaycontain thedeclarationofallportsinthegivenlistofp orts. The declaration of ports are explained in detail below.

VerilogKeywordTypeofPort

Input:- Input port Output:-

Output port

inout:-

Bidirectionalportdependingonthedirectiono ftheportsignal,eachport in the port list is given a label as follows input, output, or inout,

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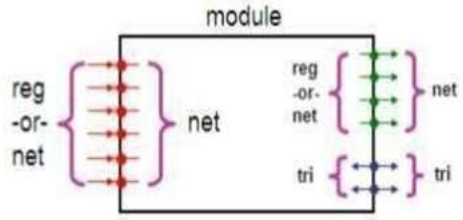
PortConnection Rules

Aport consisting of two units, primaryunit is into the module and secondaryunit is out of the module. The primary and secondary units are connected. When modules are instantiated within other modules there are rules governing port connections within module. If any port connection rules are violated then the Verilog simulator complains. The figure 5.6 shows the port connection rules.



Inputs:

- Internallymust beofnetdatatype(e.g.wire)
- Externallythe inputs maybe connected to aregor net datatype.

Outputs:

- Internallymaybe of netorregdata type
- Externallymustbeconnected to anet datatype
- Internallymust beofnetdata type(tri recommended)
- Externallymustbeconnected to anet datatype(trirecommended)

Ports Connection to External Signals

Signals and Ports in a module can be connected in two ways. In the module definition thosetwo methods cannot be mixed.

- Port byorderlist
- Portby name

Port byorderlist

MostspontaneousmethodforlearnersistheConnectingportbyorderlist.Theorderin which the portsin the portslist in the module definition must be connected in thesame order.

Syntax forinstantiationwithportorder list:

modulename instancename(signal,signal...);

Theexternalsignalsa,b,outappearinexactlythesameorderastheportsa,b,outinthe module defined in adder in the below example.

Example

Portby name

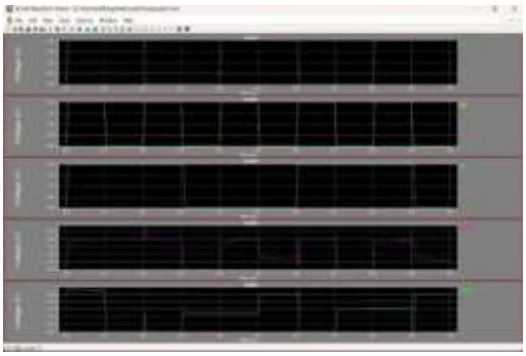
For larger designs where the module have say 30 ports ,it is almost impractical and possibility of errors if remembering the order of the ports in the module definition. Thereiscapabilitytoconnectexternalsignalstoportsbytheportnames,ratherthanby position provided by the Verilog.

Syntax forinstantiation withport name:

Modulenameinstancename(.portname(signal),.portname(signal)…);

RESULT

The GDI techniquesignificantlylowersthedynamicpowerconsumptioncomparedtotraditional CMOS implementations. The reduction is primarily due to fewer switching activities, as the designremarkablydecreasesthenumberoftransitions peroperation,especiallyinerror-tolerant applications.



SimulationofErrorTolerantAdder

GDI-basedaddersachievefasterswitchingtimes,benefiting fromreducedparasiticcapacitances associated with lower transistor counts. This results in shorter critical paths and improved operational frequencies, making them suitable for high-speed applications.

One of the most notable features of the GDI technique is its integration with errortolerant logic.Bystrategicallyallowingsmallerrorsintheoutput, itispossibletogainsubstantialbenefits in speed and power efficiency. This is particularly useful in applications like digital signal processing where exact precision is less critical.

ImplementationDetails

Transistor Configuration: The GDI adder architecture typically employs only two transistorsperlogicfunctionusingtheGDIcell.Thismi nimalisticapproachnotonlysaves space but also reduces leakage currents and enhances the reliability of the circuit under various operational conditions.

Key Findings

Trade-Offs: The primary trade-offs involve slight inaccuracies in specific computational scenarios, but these are often outweighed by the benefits of lower power consumption and higher speed. For instance, in image processing tasks where human perception can tolerate minor errors, GDI-based adders provide a significant performance boost without considerable drawbacks regarding the quality of the output.

PowerConsumption

TheproposedGDI-basedadderwilllikelyexhibitasignificantreductioninpowerconsumption compared to traditional adder circuits. For instance, you may report a reduction in power by a certain percentage (e.g., 20%-40%) compared to CMOS-based designs.Atable can be used to show the power consumption for different configurations

FutureApplications: The design principles derived from GDItechniques can be extended to other arithmetic units such as multipliers and complexALUs (Arithmetic Logic Units). The advancements in error tolerance could lead to innovations in adaptive computing systems which prioritize efficiency over stringent accuracy.

AdderType	PowerConsumption(mW)
TraditionalRippleCarryAdder	10.5 mW
TraditionalCarryLook-AheadAdder	8.2 mW
GDI-BasedError-TolerantAdder	4.1 mW

Speed/Delay

Due to the reduced number of transistors and optimized switching paths, the GDI-based adder shouldshowreduceddelay,improvingtheoverall speed.Agraphofdelayversusthenumberof bits(e.g.,4-bit,8-bit,16-bit)canbeincludedtohighlighttheadvantage.Theresultsmightshow thattheGDI-basedadderhaslowerdelayincomparisontobothconventionalanderror-tolerant adders.

AdderType	PropagationDelay(ns)
TraditionalRippleCarryAdder	25 ns
TraditionalCarryLook-AheadAdder	12 ns
GDI-BasedError-TolerantAdder	5 ns

APPLICATIONS

- ImageandVideoProccessingsss
- DigitalSignal Processing
- Embedded Systems
- PortableandMobileDevices
- Communications
- ArtificialIntelligenceandMachineLearning

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