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A study of Enhancement in Power Consumption and Energy Efficiency Using Bandwidth Scheduling

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ABSTRACT

The transfer of big data in various applications across high-performance networks (HPNs) in anationalorinternationalscopeconsumesasignificantamountof energy onadailybasis.However, most existing bandwidth scheduling algorithms only consider traditional objectivessuch as data transfer time minimization, and very limited efforts have been devoted to energyefficiency in HPNs. In this paper, we consider two widely adopted power models, i.e. power-down and speed-scaling, and formulate two instant bandwidth scheduling problems to minimizeenergy consumption under data transfer deadline and reliability constraints.The model showsthat today the access network dominates the Internet's power consumption and, as access speeds grow, the core network routers will dominate power consumption. The power consumption ofdata centers and content distribution networks is dominated by the power consumption of datastorage for material that is infrequently downloaded and by the transport of the data for materialthat is frequently downloaded. Based on the model several strategies to improve the energyefficiency of the Internet are presented.The performance superiority of the proposed solutions is illustrated by extensive resultsbased on both simulated and real-lifenetworks in comparisonwithexistingmethods.

KEYWORDS:High-performancenet works,bandwid the scheduling,energy efficiency.

1. INTRODUCTION

The Internet has become an integral component of the economies of all developed and developing nations. The virtual cycle of improvements in telecommunications supporting economic growth, which, in turn, supports growth in telecommunications infrastructure has served many nations very well. However, this cycle cannot continue without end because all telecommunications networks require resources to function, particularly (electrical) power, to operate. The larger the network becomes (in both capacity and physical size) the more electrical power it consumes. Today the information and telecommunications sector is responsible for approximately 5 percent of the total electrical power consumption in developed national economies [1]. The Internet's infrastructure consumes approximately 1 percent of a developed nation's total electricity consumption in these countries [2–5]. This percentage will grow as higher-speed national broadband access networks are rolled out over the coming years. The rate of growth of the Internet, in terms of both uptake and capacity increase, means that actually reducing its total power consumption is unlikely to be a realistic goal. The network is growing too fast. A more practical goal is to improve the energy efficiency of the Internet. By energy efficiency we mean the amount of data that could be conveyed from end to end per quantum of energy consumed by the network. This measure of energy efficiency is simply the reciprocal of the energy per bit of data transported and/or processed. Note that although we identify those parts of the Internet that dominate its power consumption (i.e., watts or watts/user), we discuss methods for improving energy efficiency (i.e., reducing Joules per bit). The relationship between these two quantities is power consumption (watts) is equal to energy efficiency (Joules per bit) multiplied by the traffic volume (bits per second). We adopt this approach because the Internet is a complex engineering structure, and any attempt to improve the overall energy efficiency is best focused on those parts that consume the most power. Therefore, a key step in this process is identifying those parts.

2. CHOOSING THE RIGHT PROCESS TECHNOLOGY

Migrating to a smaller process technology node has always provided higher integration, lower power, and greater performance than the previous node, and 28 nm is no exception. The 28-nm

process delivers clear performance benefits, but to realize the full potential of these benefits, the proper flavor of the 28-nm process must be selected. Altera chose TSMC's 28-nm High-Performance (28HP) HKMG process and leveraged its seventeen-year-long relationship with TSMC to optimize the process for low power on Stratix V FPGAs. This 28HP process also allows Stratix V FPGA to provide 28-Gbps power-efficient transceivers for ultra-high bandwidth applications. The exceptional performance of the 28HP process is driven not only by the introduction of HKMG, but also by the second generation of advanced strain technology, including embedded silicon germanium (SiGe) in source-drain regions of transistors for faster circuit designs. Altera produces tensile strain in NMOS transistors through a cap layer, and compressive strain for PMOS transistors through embedded SiGe in the source and drain (see Figure 1). These strained silicon techniques increase electron and hole mobility by up to 30% and the resulting transistor performance by up to 40%. Because better performance at the same level of leakage is achieved with strained silicon, part of this performance gain is traded for reduced leakage, leading to a superior process that has faster performance and lower leakage compared to other 28-nm process options without strained silicon. No other 28-nm process flavor has this potent combination of HKMG and advanced strain available for maximum performance characteristics of devices manufactured on that process.

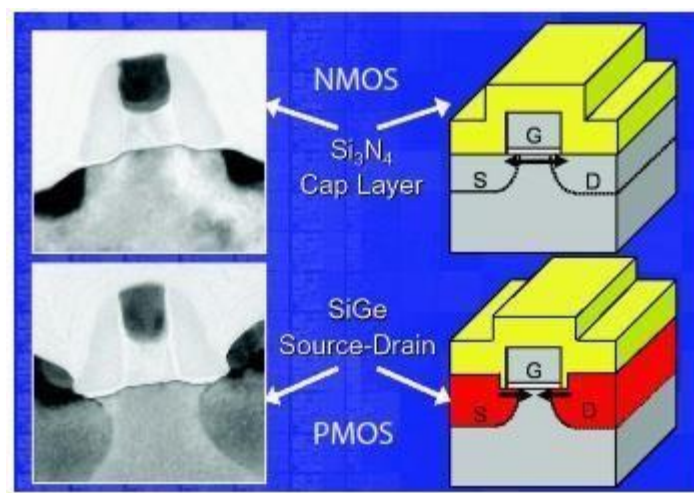


Figure 1. Strained Silicon Techniques on 28HP Process Enable Higher Performance Transistor

Altera took full advantage of the various 28HP process capabilities to reduce power and increase performance. Table 1 summarizes the various process innovations and techniques leveraged by Altera on the 28HP process to reduce static power by 25% versus the standard 28HP process from TSMC.

Table 1. Process Techniques on 28HP to Reduce Power and Increase Performance

Process Techniques on 28HP	Lower Power	Higher Performance
Custom low-leakage transistors (1)	✓	
Custom low bulk leakage (I _{bulk}) (1)	✓	
Longer channel length transistors	✓	
HKMG	✓	✓
SiGe strain (PMOS)		✓
Si ₃ N ₄ strain (NMOS)		✓
Lower capacitance	✓	✓
Lower voltage (0.85 V)	✓	

In addition, Altera leveraged the lower voltage offered by the 28HP process to significantly reduce power without impacting performance. Figure 2 shows the static power and dynamic power savings achieved by Stratix V FPGA on a 0.85-V supply (on most devices) compared to a 1.0-V supply. Static power is proportional to V_{cc}^3 , and by reducing voltage from 1.0 V to 0.85 V, the static power is reduced by 39%. On the other hand, dynamic power is proportional to V_{cc}^2 , and a voltage reduction from 1.0 V to 0.85 V leads to a 28% power reduction.

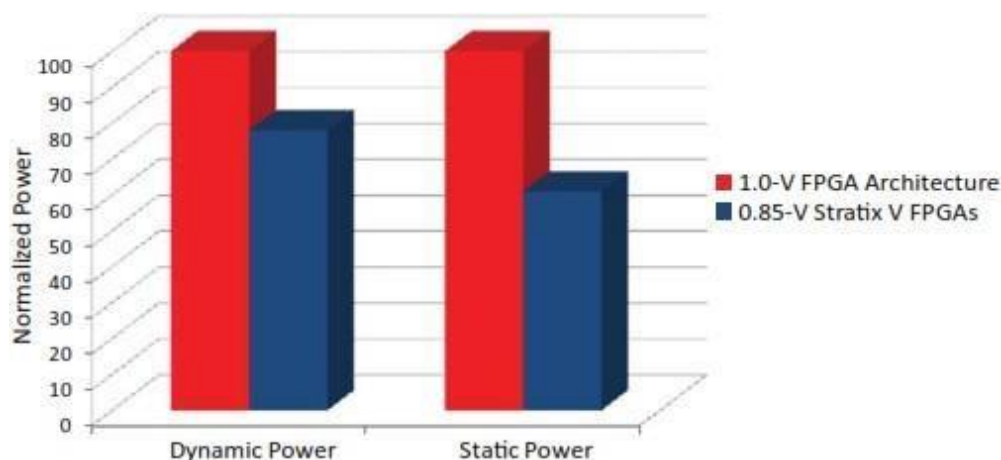


Figure2.Static and Dynamic Power Comparison for Same Architecture on Same Process at 0.85V and 1.0V

3.FPGA ARCHITECTURE INNOVATIONS

Altera has been leading the industry in introducing architectural innovations, enabling designers to lower power and increase bandwidth in their system designs. The most recent four generations of Stratix series FPGAs show a clear trend of lower power and higher bandwidth with every process node shrink. As shown in Figure 3, Stratix V FPGAs enable designers to achieve 5X higher bandwidth at 80% lower total power compared to Stratix II FPGAs. Stratix V FPGAs are based on the high-performance architecture of Stratix IV FPGAs and deliver key architectural innovations to enable designers to achieve higher bandwidth and lower power through an unprecedented level of system integration and ultimate flexibility. These innovations include the introduction of the Embedded Hard Copy Blocks, 28G transceivers, and partial reconfiguration. Stratix V FPGAs continue to leverage the highly successful Programmable Power Technology used in Stratix III and Stratix IV FPGAs.

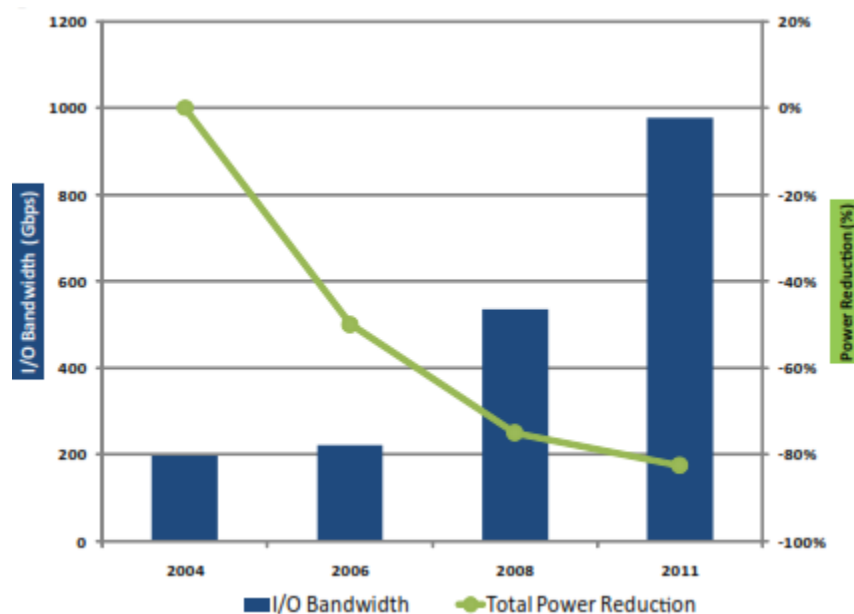


Figure3.Power and Bandwidth Trends in Stratix Series FPGAs

4. HIGH-BANDWIDTH, POWER-EFFICIENT TRANSCEIVERS

Another key innovation introduced by Altera on 28-nm is the power-efficient 28-Gbps high-speed serial transceivers shown in Figure 4. These 28-Gbps transceivers are designed for chip-to-chip and chip-to-module applications and targeted to address the trend in the wireline market to move to 28-Gbps in optical module interfaces.

Optical modules are used in communication and computer systems to convert electrical signals received to optical signals and then to drive them to optical fiber channels. Similarly, they convert the optical signals to electrical signals and drive them to electrical copper channels. The evolution of the optical module focuses on increasing data rates, lowering power, and reducing form factor by removing components off the module. These challenges get pushed off to silicon and system design.

Today, 100 Gigabit Ethernet (100GbE) networks are implemented with electrical interfaces utilizing a 10-lane by 10- or 11-Gbps signaling rate. Given the characteristics of the optical solutions being developed by various industry bodies, the current drive is for a narrower electrical interface with four lanes in each direction. To address this trend, 28-Gbps signaling protocols for chip-to-chip and chip-to-module applications are being created, an example being Common Electrical I/O 28 Gbps (CEI-28G). This protocol will enable smaller and more cost-effective optical modules (such as CFP2) with lower power dissipation for multiple 100-Gbps applications on a single line card.

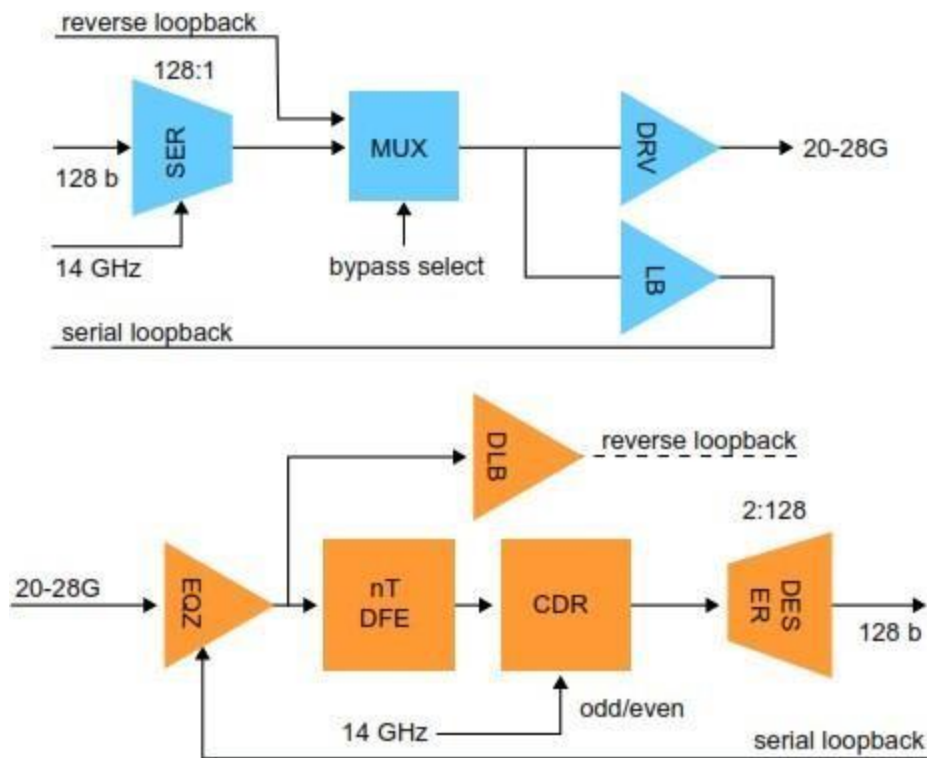


Figure 4.28- Gbps Tx and Rx Architecture in Stratix V FPGAs

With 28-Gbps transceivers, designers can reach higher bandwidth and lower power simultaneously.

Figure 5 shows two implementations of 100GbE interfaces to optical modules. In the first implementation, 10 channels, each running at 11.3 Gbps, interface with a 100G (CFP) optical module and consume 1.58 W. In the second implementation, four channels, each running at 28-Gbps, interface with next generation 100G (CFP2) optical modules, consuming half the power at 0.8 W.

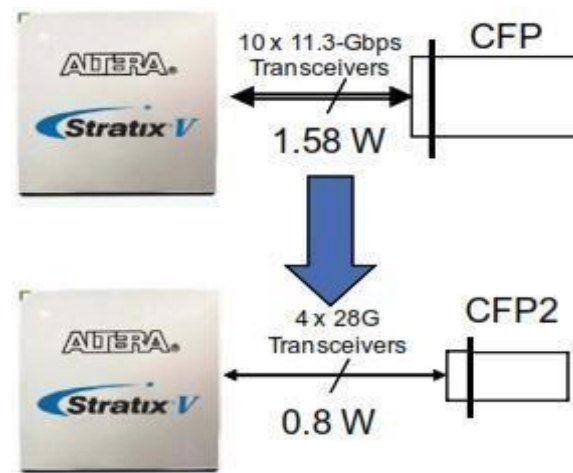


Figure 5. Increase Bandwidth and Cut Power by Half Using 28-Gbps Transceivers

In addition to 28-Gbps transceivers, Stratix V FPGAs integrate power-efficient transceivers with data rates ranging from 600 Mbps (or 150 Mbps with oversampling) to 14.1 Gbps with best-in-class signal integrity and lowest jitter. Stratix V GX FPGAs offer up to 66 identical power-efficient 14.1-Gbps transceivers that provide up to 44 independent data rates through independent clock sources. The 28-Gbps and 14.1-Gbps transceivers in Stratix V FPGAs are power efficient across all supported data rates. Altera took every effort to ensure that transceivers in Stratix V FPGAs deliver the required high bandwidth or data rate at the lowest power. Specifically, Altera introduced transceiver power supply banking (see Figure 6) in Stratix V FPGAs, where the transceivers are powered with one of the following power supply voltage options depending on the transceiver usage in various applications:

- Low power (0.85 V) configuration—Used for data rates of Gbps in short reach, chip-to-chip, and chip-to-module applications with basic equalization techniques, such as transmit pre-emphasis/de-emphasis and continuous time linear equalizer (CLTE).
- High performance (1.0 V) configuration—Used for noisy and lossy channels, such as long-reach and backplane applications at data rates of >6.5 Gbps. It includes more advanced equalization circuit blocks, such as decision feedback equalization (DFE) and automatic dispersion compensation engine (ADCE), in addition to basic linear equalization circuits.

- Off(0 V)—Used to power down unused transceivers to save power.

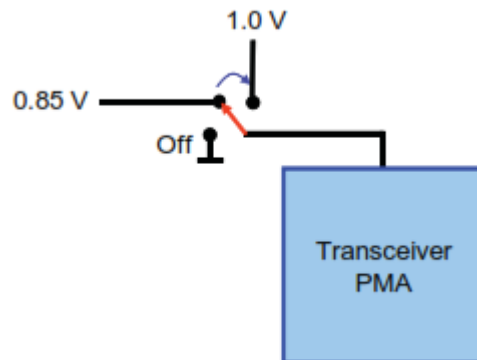


Figure 6. Three Power Supply Voltage Options for Stratix V Transceivers

In addition to transceiver power-supply banking, Altera leveraged various design techniques to ensure Stratix V transceivers are power efficient. These techniques include the use of ultra-low jitter LC-PLL technology supporting low power at the highest data rates in addition to transistor body biasing to reduce static power, and clock gating to minimize dynamic power. As a result, Stratix V transceivers deliver best-in-class signal integrity performance at the lowest power. Figure 7 shows the transceiver power per channel (blue bars) and the transceiver power per gigabit (red line) for varying data rates on Stratix V FPGAs.

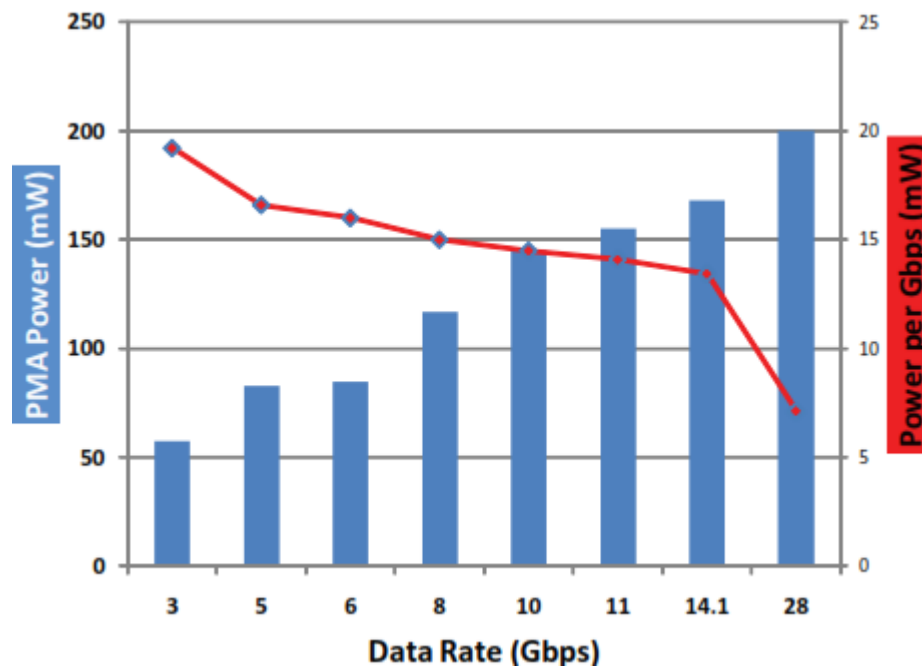


Figure 7. StratixV Transceiver Power per Channel and per Gbps

At 28-Gbps, the PMA power per transceiver channel is 200 mW or 7 mW per Gbps. By going to higher data rates, designers can reduce their system power significantly. For example, to build a 10G interface, designers can choose one of the following:

- Four XAU I channels—Each running at 3.125 Gbps, consuming 240 mW
- One 10G channel—Running at 10.3125 Gbps, consuming 145 mW, or 40% lower power

5. CONCLUSION

Power-down and speed-scaling, for minimizing energy consumption of data transfer under deadline and reliability constraints. Both of the problems have been proved to be NP-complete. Altera is addressing the requirements of next-generation applications pushing the limit for higher bandwidth and lower power by introducing key innovations on 28-nm Stratix V FPGAs, including:

- 28HP process innovations

- ProgrammablePowerTechnology
- Lower voltage(0.85-V)architecture
- High-bandwidth,power-efficienttransceivers
- EmbeddedHardCopyBlocksandextensivehardening ofIP
- Hardpoweringdownoffunctionalblocks
- I/Oinnovationsenablingpower-efficientmemoryinterfaces
- QuartusIIsoftwarepoweroptimization
- LogicandRAMclockgating
- Fewer powerregulators,switching regulatorsonallsupplies
- Board-levelintegration:oscillators,decouplingcapacitors,OCT
- Easy-tousepartialreconfiguration

Altera's comprehensive approach rewards Stratix V customers with many benefits including higher performance and lower power FPGA, higher integration through extensive hardening of IP, and ultimate flexibility through easy-to-use partial reconfiguration. Stratix V FPGAs are the ideal devices for high-end applications requiring high bandwidth and lower power.

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